CT & DH Subsystem

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Mission Requirements (1 of 2)

From Mission Requirements Document (MRD), Section 3.7.1.1.1.2:

- **Provide the Capability to Decode, Authenticate and Process Unencrypted CCSDS Commands Received Via the Uplink**
- **Execute Critical Commands Without CPU Interaction**
- **Execute Stored Commands**
- **Distribute Commands to All Subsystems**
- **Provide Capability to Transfer Specific Uplink Data to Processor for Control and Reprogramming**
- **Collect State-of-Health (SOH) Telemetry From All Subsystems**
- **Collect, Store, and Buffer Instrument Science Data**
  - **Memory Size: 4 Gbits**
  - **Maximum Data Rate of 12.5 Mbps**
  - **Average Rate of 320 Kbps**
- **Store Science and Telemetry Data During Downlink Outages**
- **Provide for CCSDS Downlink Capability of up to 500 Kbps of Science and Telemetry Data**

Mission Requirements (2 of 2)

From Mission Requirements Document (MRD), Section 3.7.1.1.1.2:

- **Provide Error Control Coding , Interleaving, and Randomization to Downlink Data Stream**
- **Maintain Spacecraft Time**
- **Provide Capability to Synchronize Instrument Counter, Spacecraft Time and Universal Time to Within 1 msec**
- **Manage Vehicle Attitude for Successful Mission Orbit Insertion, Stabilization, and De-Orbit**
- **Provide for an Interface to EAGE for Initial Integration**
- **Support T-Minus Zero (T0) Interface to the Launch Vehicle**
- **Provide Data and Control Interface to Instrument**

Derived Requirements

- **D1. Provide Alternate Boot EEPROM Capability in FSC (From Flight Software)**
- **D2. Provide 1 Gbyte Star Catalog Memory (From Flight Software)**
- **D3. Provide Motor Control Signals (From EPS and Mechanisms)**
- **D4. Provide Redundant System (From Systems Engineer)**

CTDH Subsystem Trades

- Spacecraft I/O Options
  - Develop Custom Spacecraft I/O Card
  - Use Remote Interface Unit (RIU)
  - RIU Chosen (BF Goodrich, RIU Expanded Model)
    - Lower Risk - No Development Necessary
    - Allows Software Reuse From ICM
- Processor
  - FSC Processors
    - RHC-3001
    - Rad6000
    - PowerPC
  - FSC Processor Chosen
    - RHC-3001
      - Software Re-use From ICM
      - Existing Development Environment

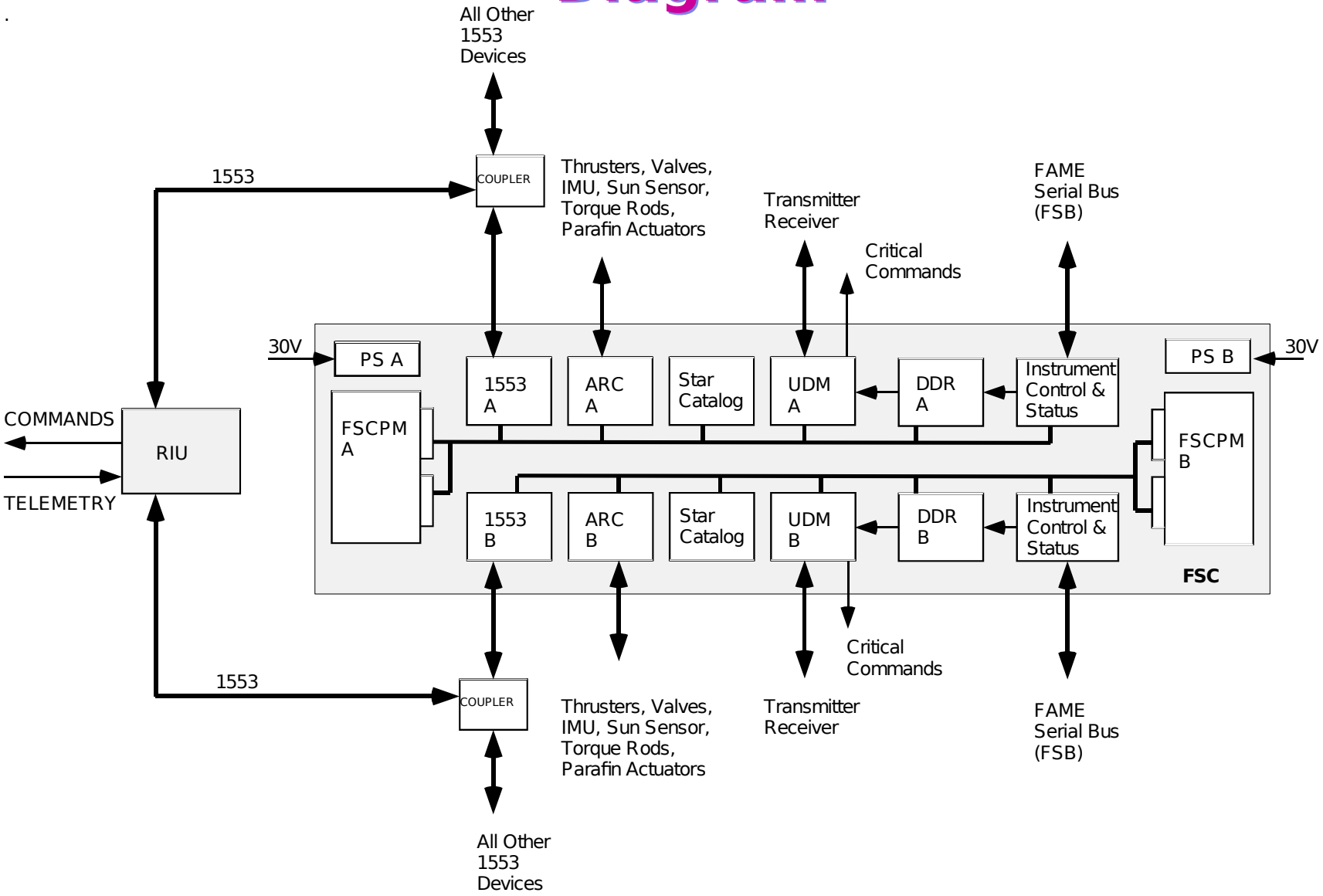
Functional Allocation (1 of 2)

- Remote Interface Unit (RIU)
  - Provide Non-Critical Command Capability Via 1553
  - Provide Telemetry Gathering Capability Via 1553)
- Fame Spacecraft Controller Processor Module (FSCPM)
  - Processing for ACS Maneuvers
  - Stored Command Execution
  - Provide On-Board Processing for Instrument Control
- 1553 Card
  - Provide VME Bus Accessible Control of Redundant 1553 Buses
  - Provide Non-Volatile Memory for Alternate Boot
- Attitude and Reaction Control (ARC) Board
  - Provides Drivers for:
    - Eight Thrusters
    - Three Torque Rods
    - Four Paraffin Heaters
    - Open/close for One Latch Valve
  - Provide Data Collection and Storage Interfaces for:
    - 2 Inertial Measurement Units (IMU)
    - 2 Sun Sensor Instruments

Functional Allocation (2 of 2)

- **Star Catalog Memory Board (SSMB)**
  - **Provide 1 Gbyte VME Accessible Memory for Star Catalog**
- **Uplink/downlink Module (UDM)**
  - **Execute Critical Commands Without CPU Interaction**
  - **Pass All Commands to CPU**
  - **Provide CCSDS Formatting to Downlink Stream**
  - **Provide Reed-Solomon Coding, Interleaving, and Randomization**
  - **Provide Time-Tag Capability to Correlate Instrument Clock With UTC**
  - **Provide Following Downlink Data Rates: 1, 2, 8, 16, 250 and 500 Kbps**
  - **Provide Low-Level Motor Control Via Register Controlled off the VME Bus**
- **Digital Data Recorder (DDR) Board**
  - **Provide 4 Gigabits Buffer Memory for Instrument Data**
- **Instrument Control Interface (ICI) Board**
  - **Multiplex 3-1D Window Data Channels to the DDR**
  - **Receive and Buffer 3 Independent 2D/Raw Window Data Channels**
  - **Provide Control 3 Independent Control Channels**

CTDH Subsystem Block Diagram



RIU Characteristics

- **B.F. Goodrich Remote Interface Unit, Extended Version**

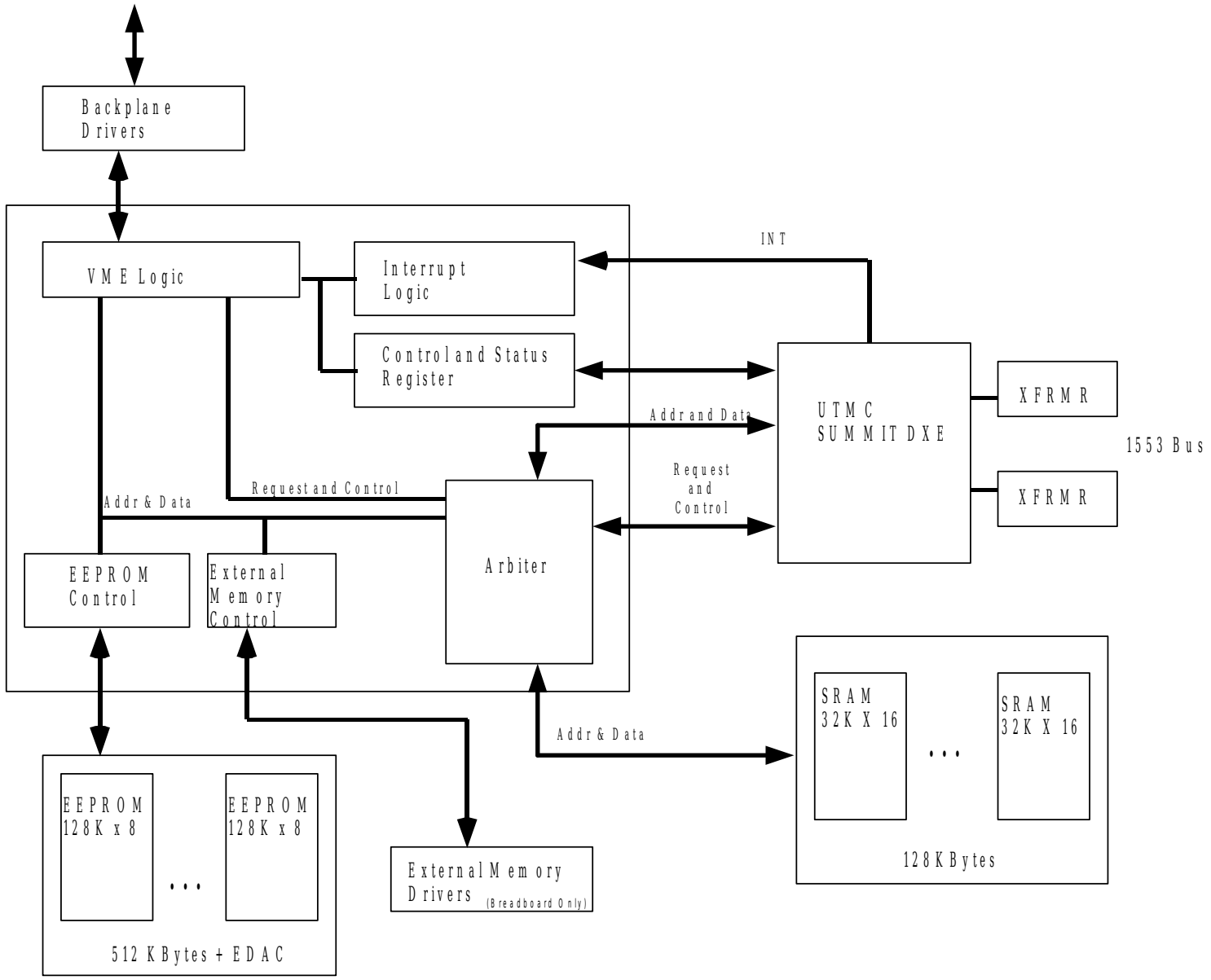
- **Telemetry Capabilities**
  - **128 Active Analog Telemetry Points, 108 Currently Assigned**
  - **128 Passive Analog Telemetry Points, 64 Currently Assigned**
  - **128 Bi-Level Telemetry Points, 58 Currently Assigned**
  - **24 Serial Telemetry Channels, 0 Currently Assigned**

- **Command Capabilities**
  - **128 High Level Commands, 104 Currently Assigned**
  - **64 Low Level Commands, 24 Currently Assigned**
  - **16 Serial Commands, 0 Currently Assigned**

FSCPM Characteristics

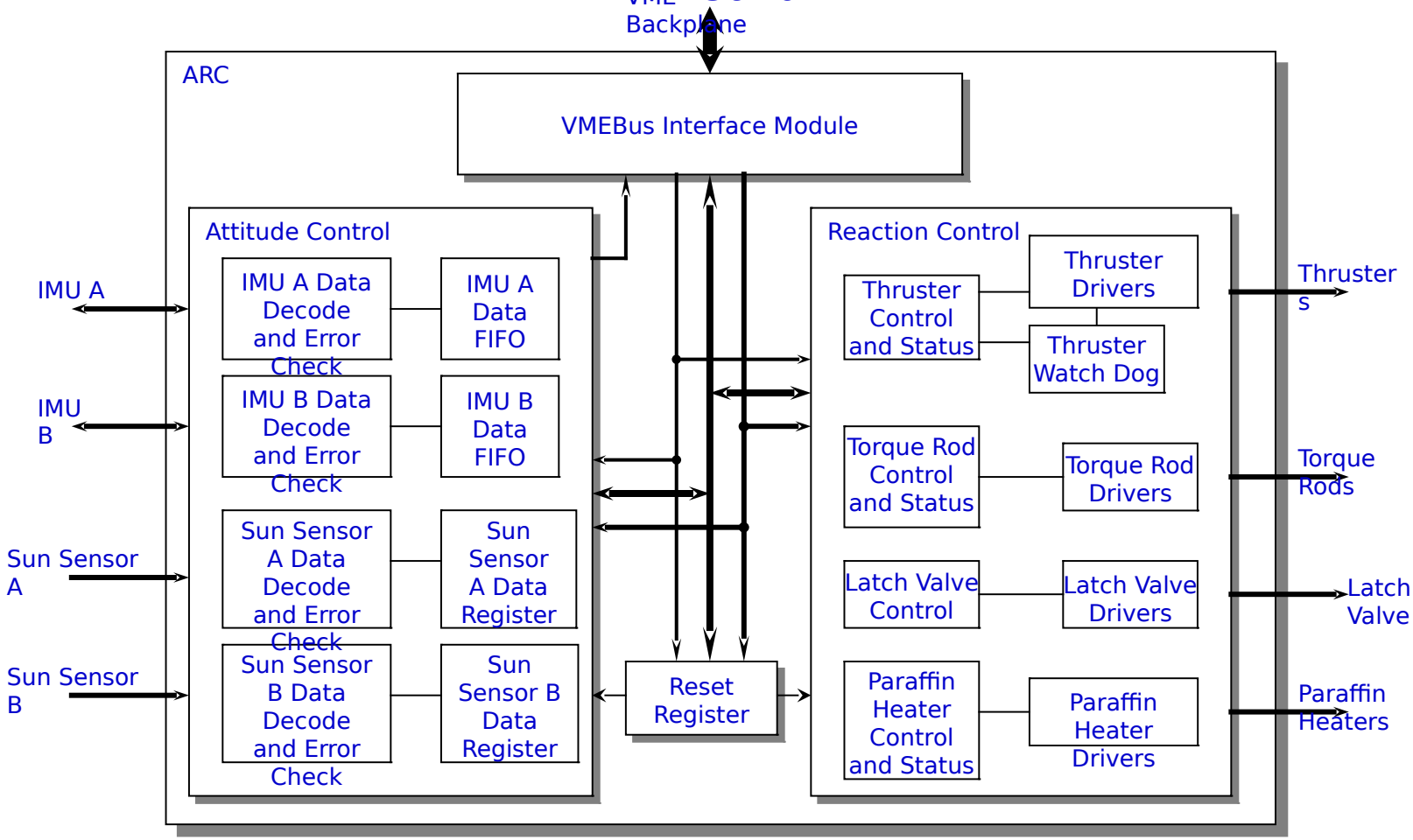
- **The Processor Chosen Is the RHC-3001 From Harris Corp**
  - **20 MHz Operation**
  - **64 Mbytes of RAM**
  - **512 Kbytes of Boot EEPROM**
  - **512 Kbytes of Instruction Cache**
  - **512 Kbytes of Data Cache**
  - **32-bit VME Interface**
  - **In Production**
  - **Heritage From Interim Control Module (ICM) Program**

1553 Block Diagram

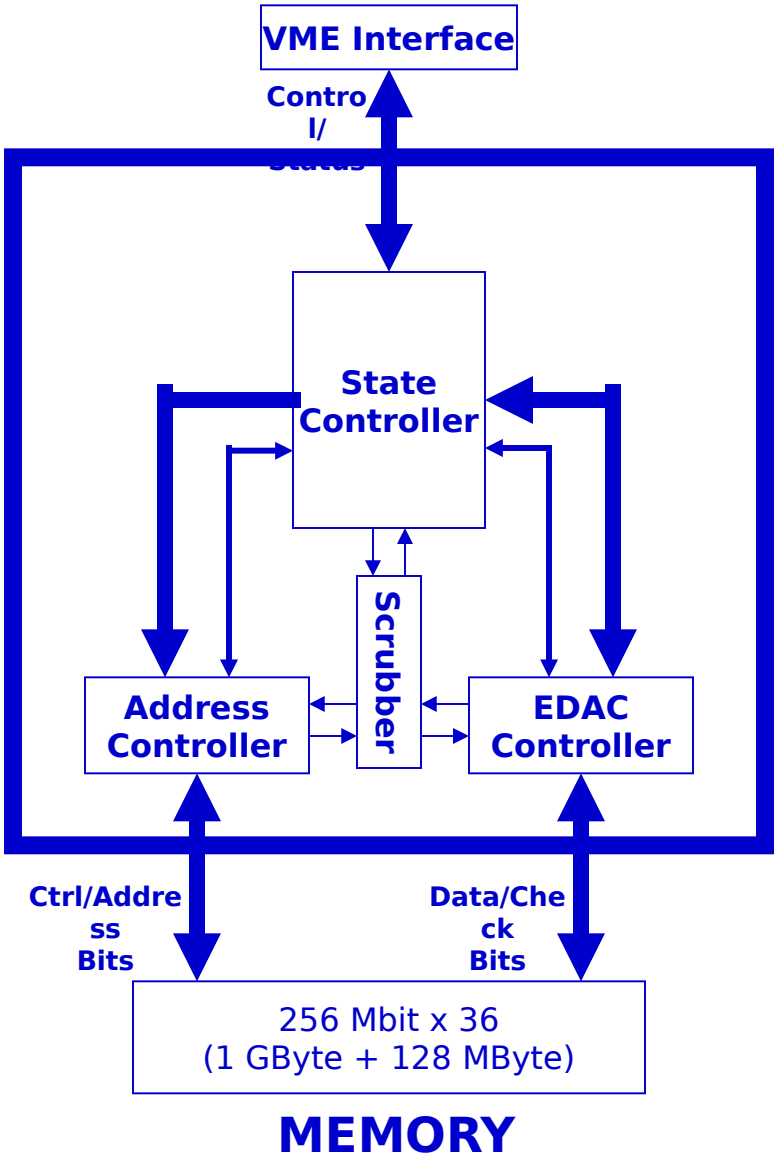


ARC Block Diagram

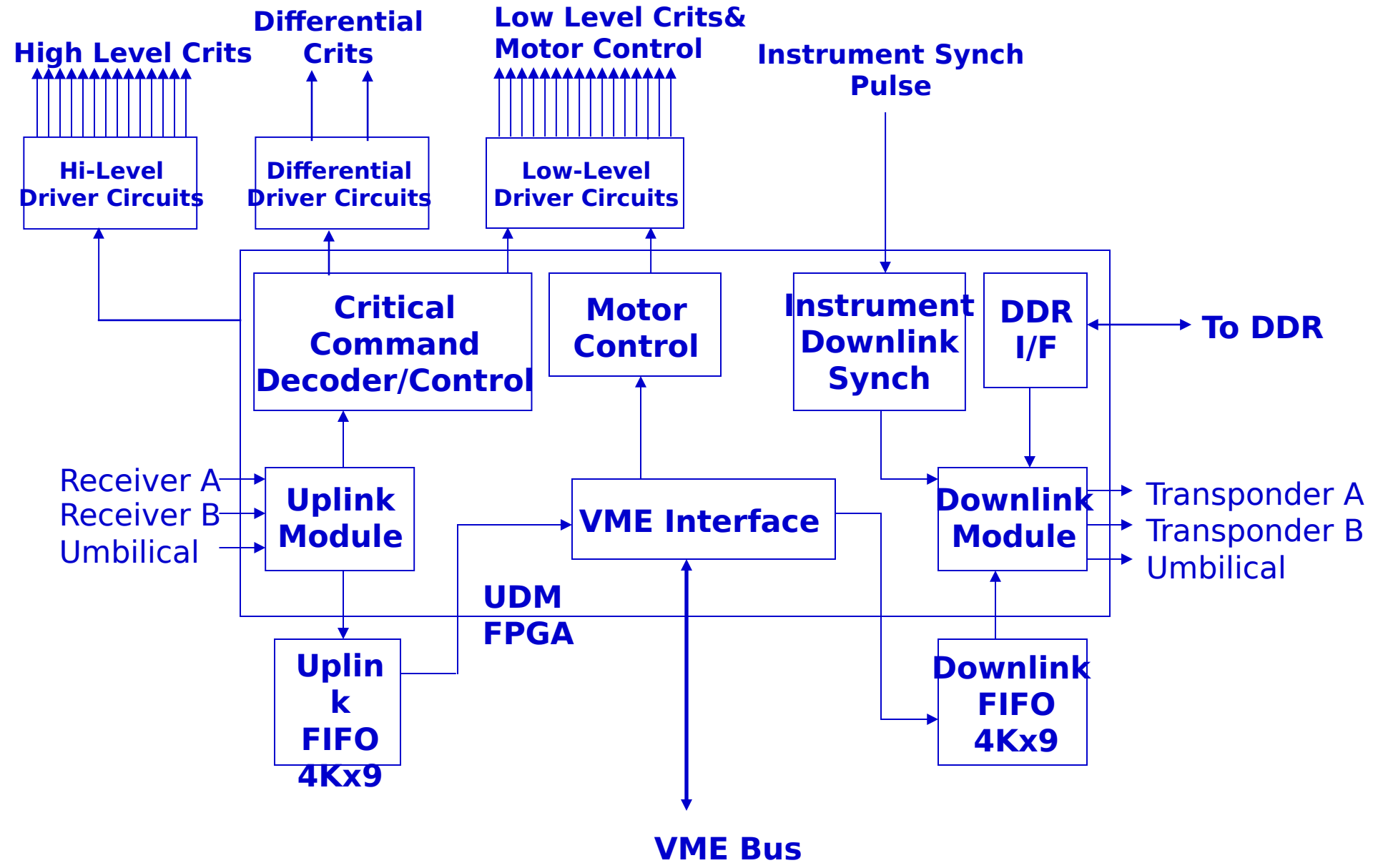
Attitude and Reaction Control Board



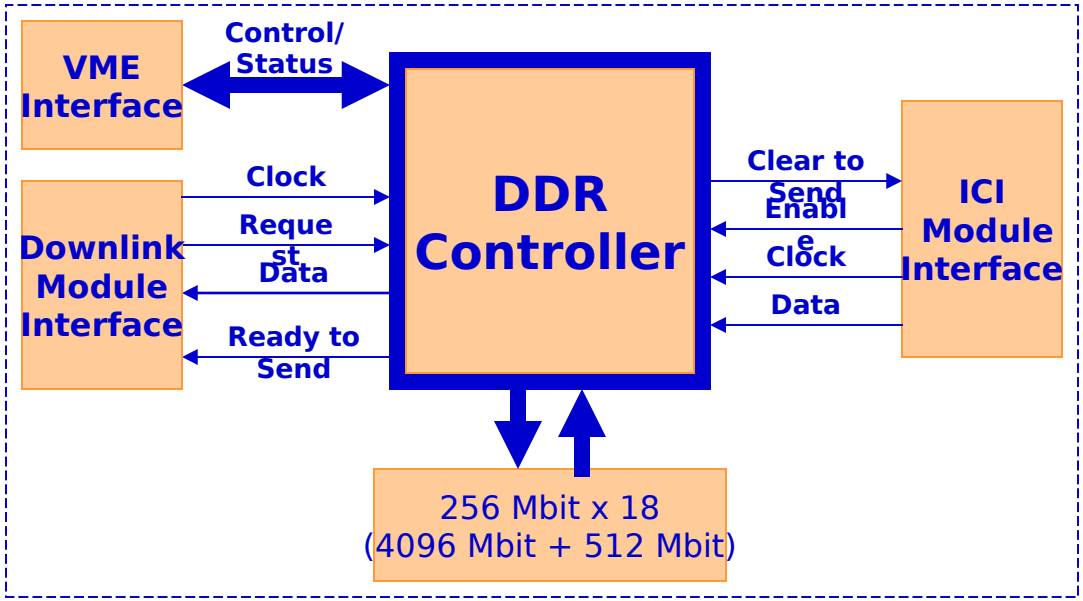
SCMB Block Diagram



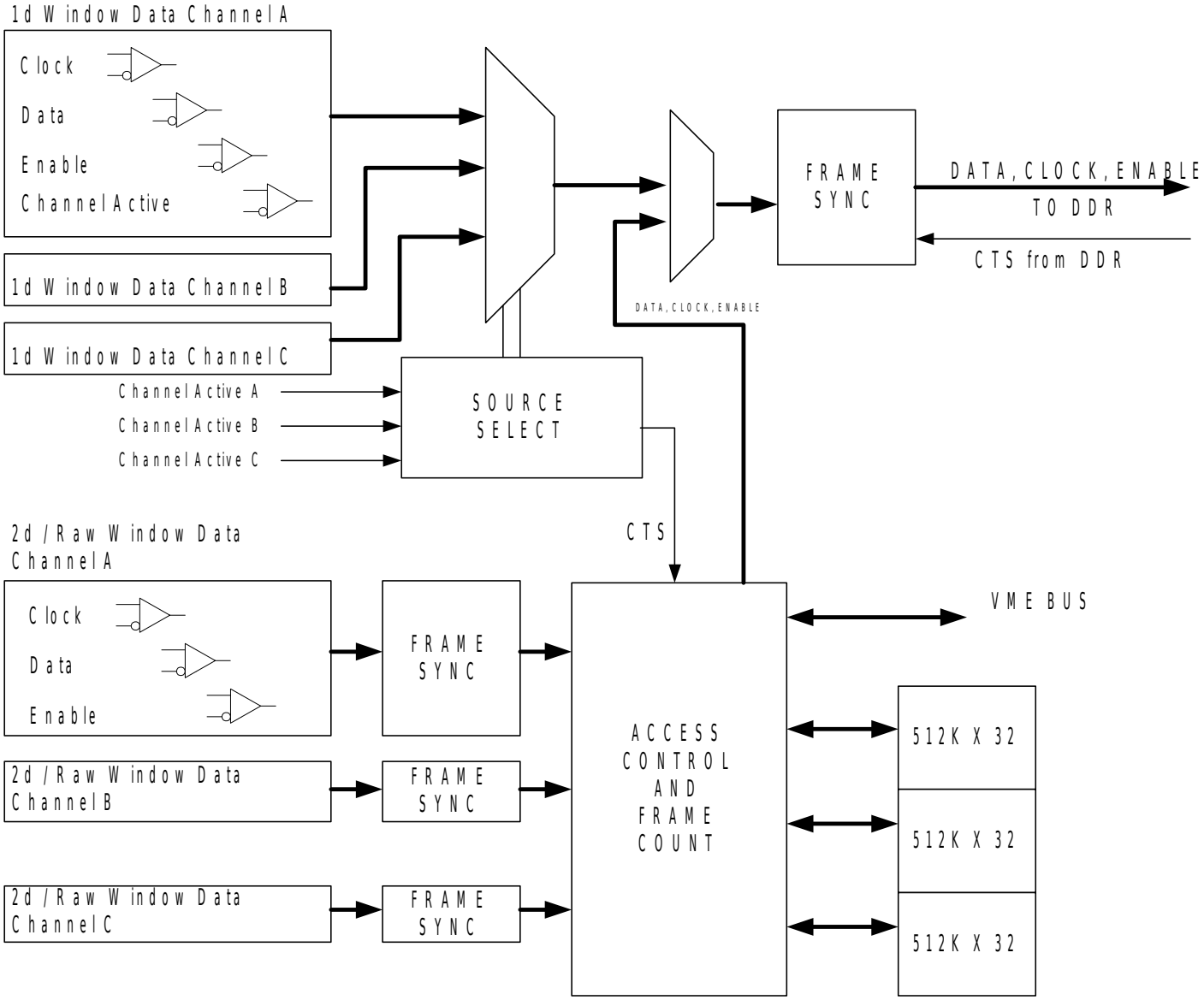
UDM Block Diagram



DDR Block Diagram

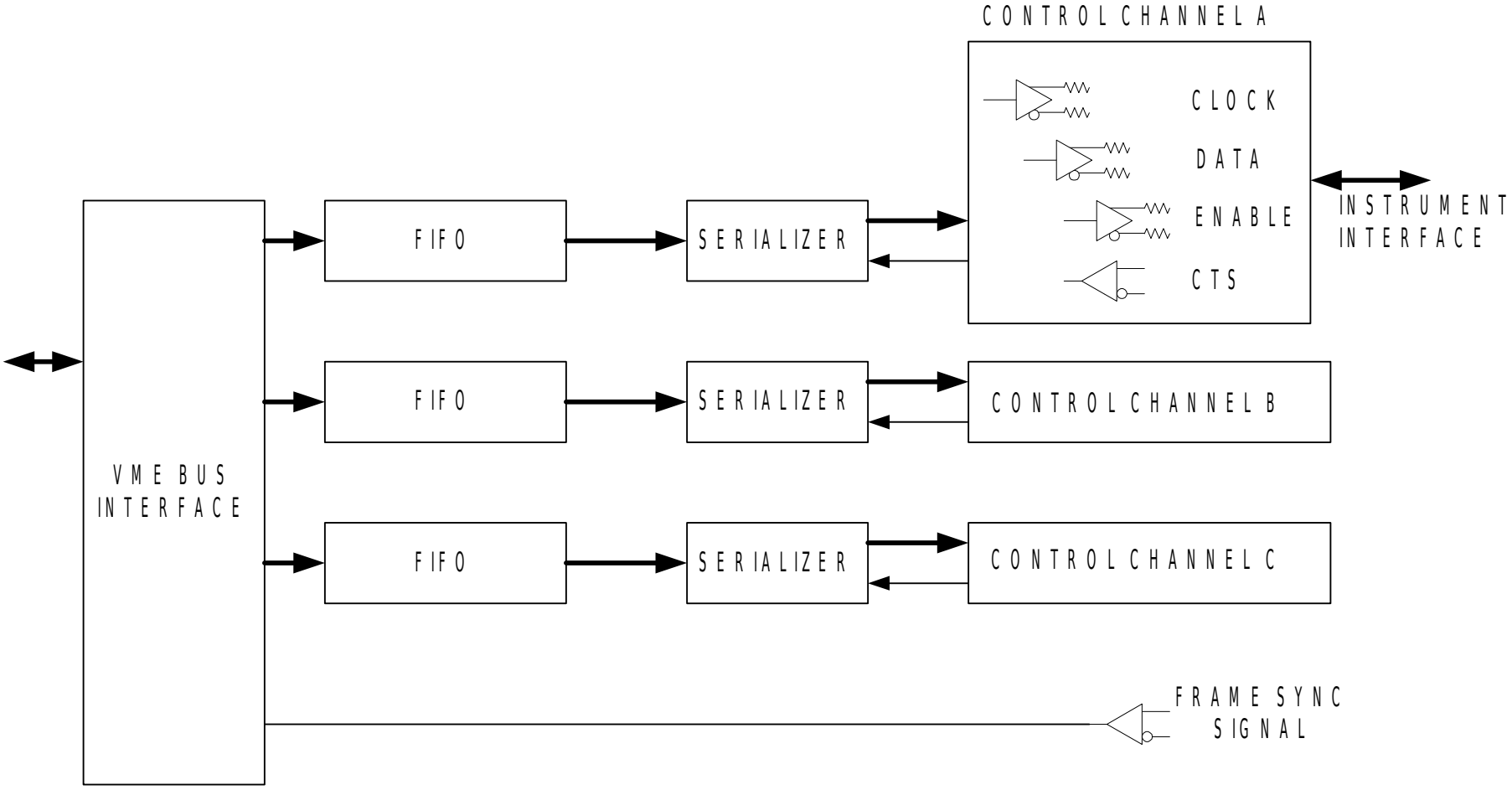


ICI Block Diagram (1 of 2)

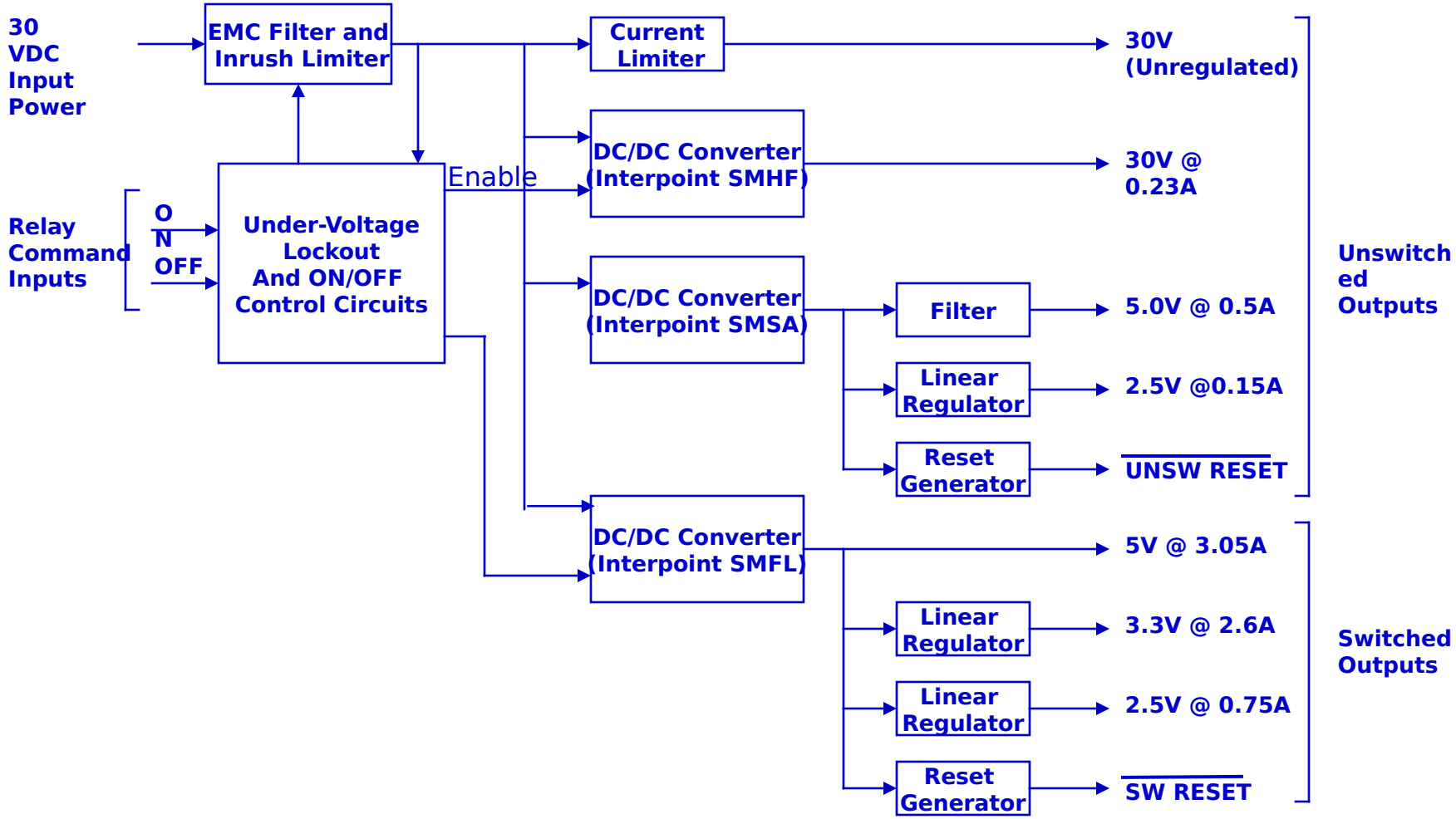


ICI Block Diagram (2 of 2)

Instrument Control Interface

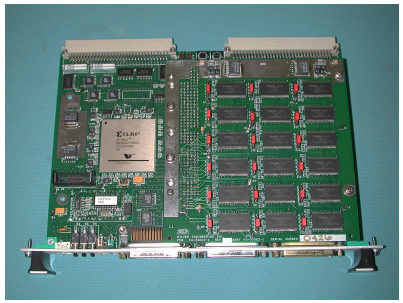


FAME FSC Power Converter Block Diagram

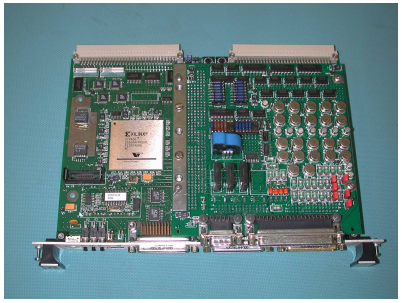


FSC Breadboard Concept

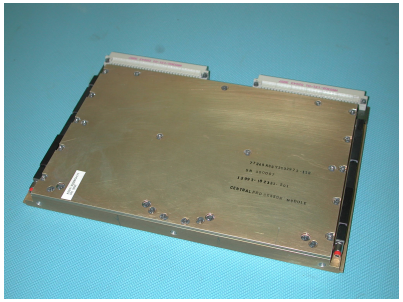
- **Breadboards Were Developed Around a Xilinx Device**
- **Circuits Were Designed Using VHDL**
  - **Circuit Designs Were Constructed With the Flight Target Device in Mind, Actel 54SX**
  - **Parallel Synthesis Operations Were Conducted to Insure Fit to Flight Device**
- **Four of Seven Breadboards Are Functional: DDR, ARC, 1553, and Processor**
  - **UDM, SCMB, and ICI Are Under Development**



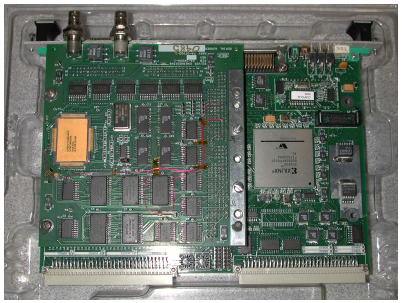
DDR



ARC



Processor



1553

Development and Integration Flow

Breadboard #1 (Single String) → **Engineering Development (Until 3/11/02)**

Available for Software Development 3/11/02

Breadboard #2 (Single String) → **Available for Instrument Interface Checkout 4/1/02**

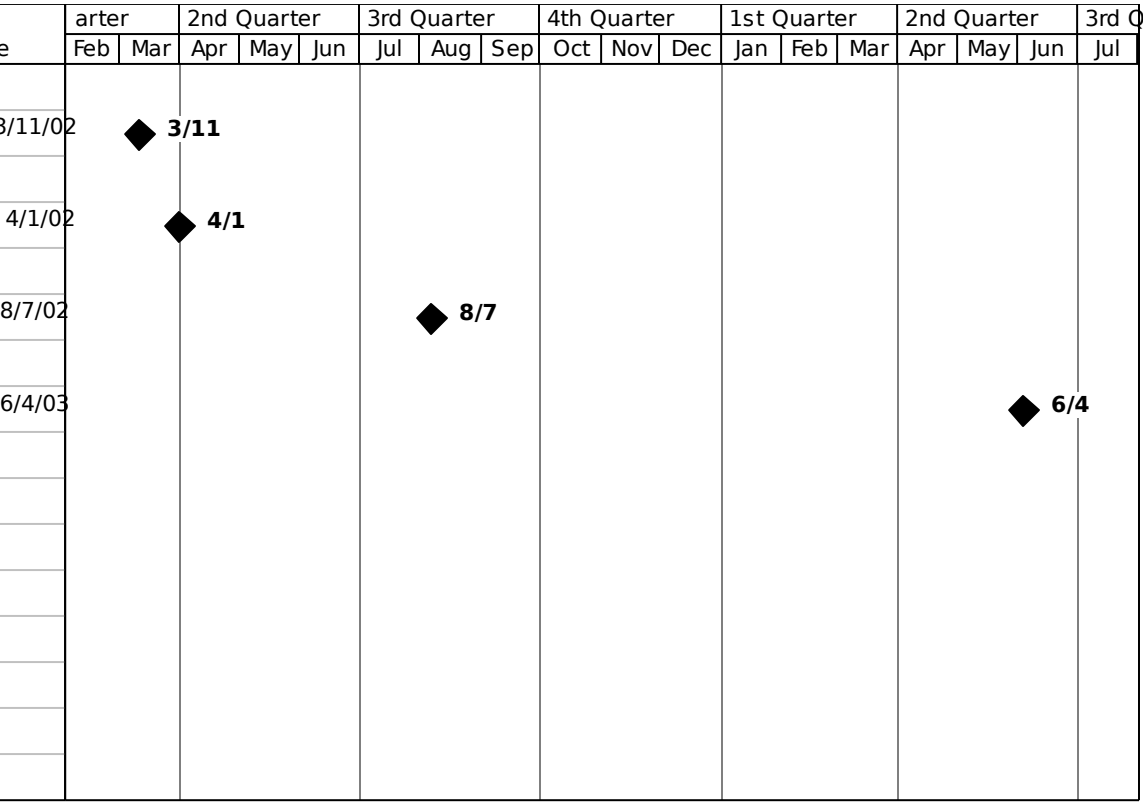
Engineering Model → **Ready for Deck Testing 8/7/02**

Available for Software Development 6/4/03

Flight Model → **Delivery to Spacecraft 6/4/03**

CT&DH Milestones

Milestone	Date
Breadboard #1 Complete	Mon 3/11/02
Breadboard #2 Complete	Mon 4/1/02
Engineering Model Ready for Deck Testing	Wed 8/7/02
Flgiht Model Ready for Integration	Wed 6/4/03



Backup

RIU Commands

	Available		Consumed		Spare
		Total Available	Total Consumed		Spares
Total Available Primary HLCs	128	128	104		24
Total Available Secondary HLCs	128				
Total Available Primary LLCs	64	64	24		40
Total Available Secondary LLCs	64				
Total Available Primary Serial Commands	16	16	0		16
Total Available Secondary Serial Commands	16				

- **HLC = High Level Commands: 28 V, 44 msec**
- **LLC = Low Level Commands: Open Collector, 192 usec**
- **Serial Commands: 16-bit Logical Shift Register**

RIU Telemetry Spares

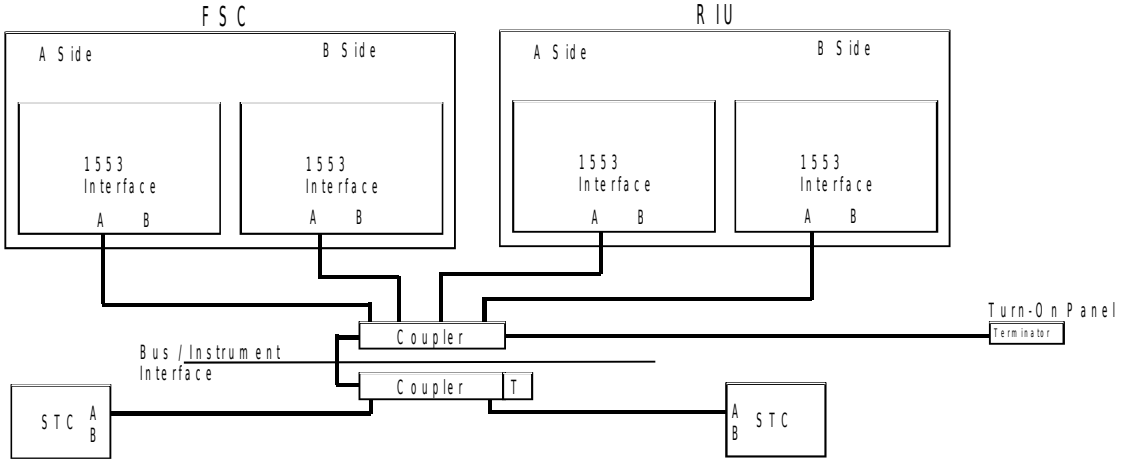
	Available		Consumed		Spare
		Total Available	Total Consumed		Spares
Total Available Primary Serial Telemetries	24	24	0		24
Total Available Secondary Serial Telemetries	24				
Total Available Primary Passive Analogs	128	128	64		64
Total Available Secondary Passive Analogs	128				
Total Available Primary Active Analogs	128	128	108		20
Total Available Secondary Active Analogs	128				
Total Available Primary Bi-Levels	128	128	39		89
Total Available Secondary Bi-Levels	128				

- **Active Analog: Reads Analog Voltages**
- **Passive Analog: Reads Thermistors and Resistance**
- **Bi-Level: Reads Logic Level Signals and Mechanical Position Indicators**
- **Serial Telemetry Channels: Reads in 16-bit Logical Shift Register**

FAME 1553 Bus Description

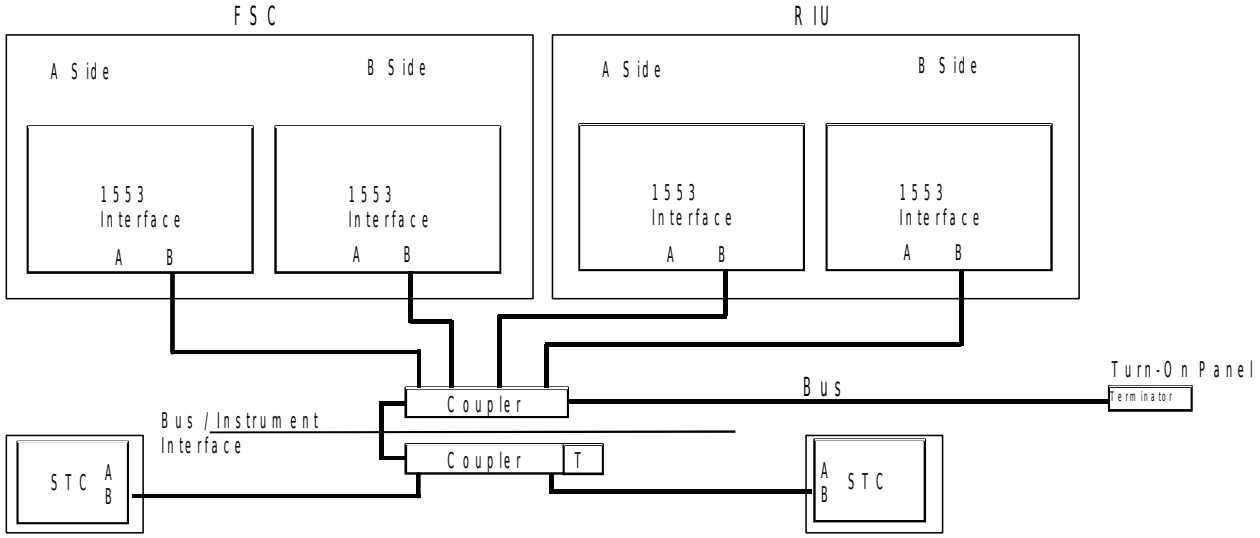
- 1553 Bus Is MIL-STD-1553B, Notice 2
- Couplers Will Contain Bus Terminations
- All Terminal Units Will Be Transformer Coupled
- All Terminal Units Will Present Redundant 1553 Busses Per Redundant Side
- All Terminal Units Will Support Auto-retry Attempts From the Bus Controller
- The FSC Will Be Bus Controller
- All Other Terminal Units Will Be Remote Terminals

1553 Cross Strapping



Bus A

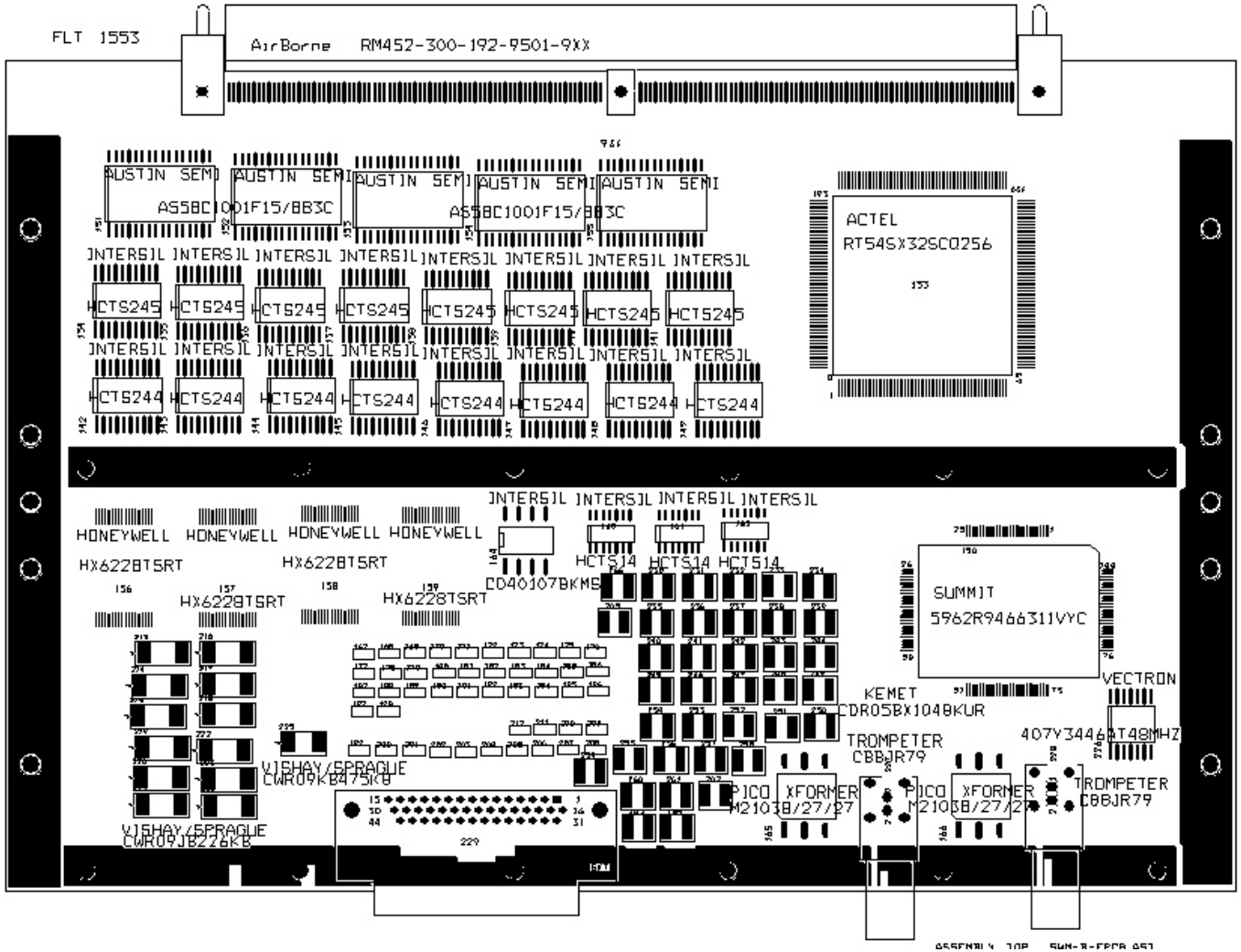
Bus B



1553 Parts List

Item	Quantity	PartNumber	Description	Manufacturer
1	12	CWR09JB226KB	Capacitor, 22UF_TANT, 20V	
2	37	CDR05BX104BKUR	Capacitor, 0.1uF, 10%, 100V	
3	1	CWR09KB475KB	Capacitor, 4.7UF_TANT	
4	2	CBBJR79		Trompeter
5	1	311P407-3S-B-12	44 socket, D Connector	AMP
6	4	RM452-300-191-9501-9xx	300 Pin Edge Connector	AirBorn
7	14	M55342K03B10E05	Resistor, 10K, 1%	
8	2	M21038/27-27	Transformer, 1553 Stub	
9	4	HX6228TSRT	SRAM, 128K X 8	Honeywell
10	1	5962R9466311VYC	Summit Chip, 1553	UTMC
11	8	M38510/65553Q*X	Bidirectional Buffer, Driver, HCTS 245	Intersil
12	5	AS58C1001F15/883C	EEPROM	Austin Semiconductor
13	3	5962R9571901Q*X	Receiver, Schmitt Trigger, HCTS14	Intersil
14	1	407Y3446AT48MHZ	Oscillator	Vectron
15	8	5962R9574401Q*X	Buffer, Driver, HCTS244	Intersil
16	1	RT54SX32SCQ256	FPGA	Actel
17	1	CD40107BKMSR	Open Collector Driver	Intersil
18	32	M55342K03B22D6R	Resistor, 22.6, 1%	

1553 Module Layout

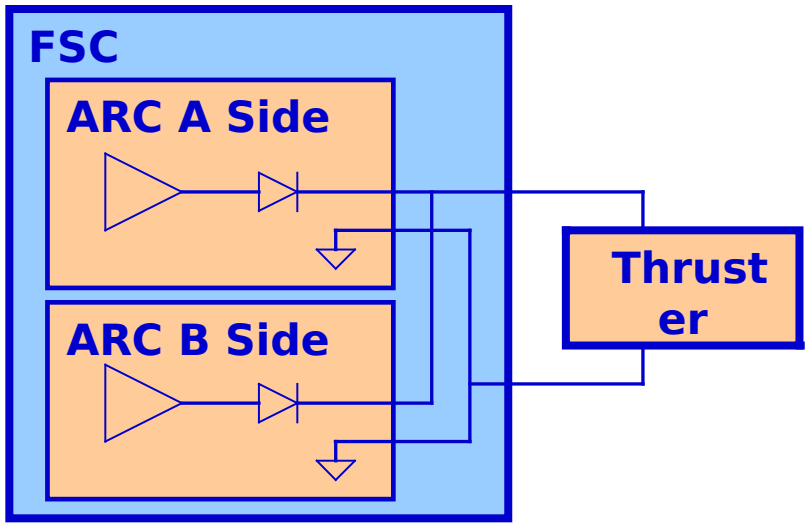


ARC Status

- **95% of Breadboard Tested and Functioning**
- **Load Simulator Completed**
- **Test Board Tested and Functioning**
- **Requirements Document Is Up-to-Date**

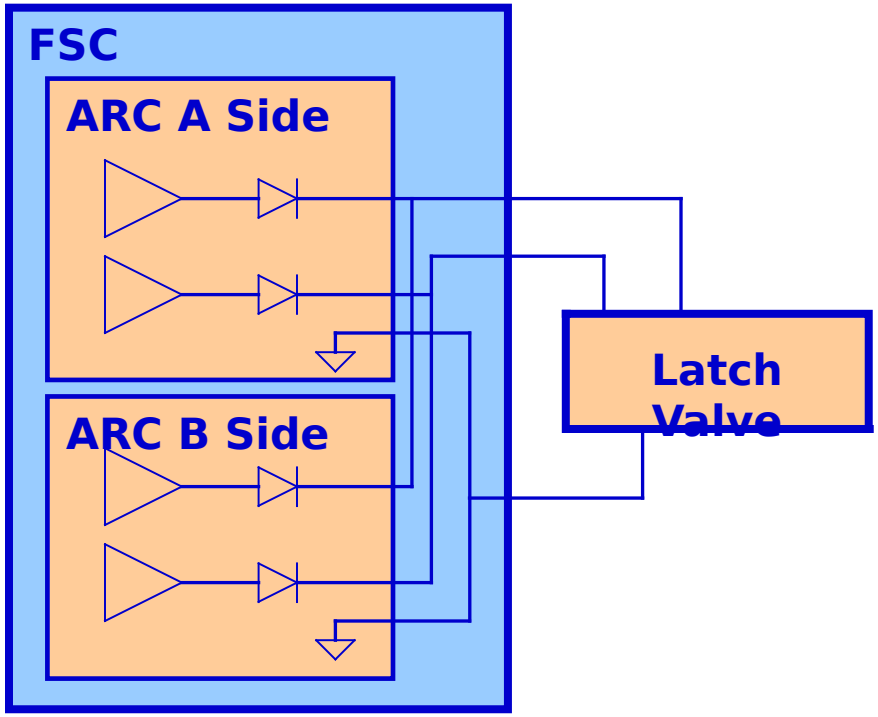
ARC Cross-Strapping 1 of 6

Thruster Cross-Strapping (One of Eight Thrusters Shown)
Requires 8 Drivers Per Side



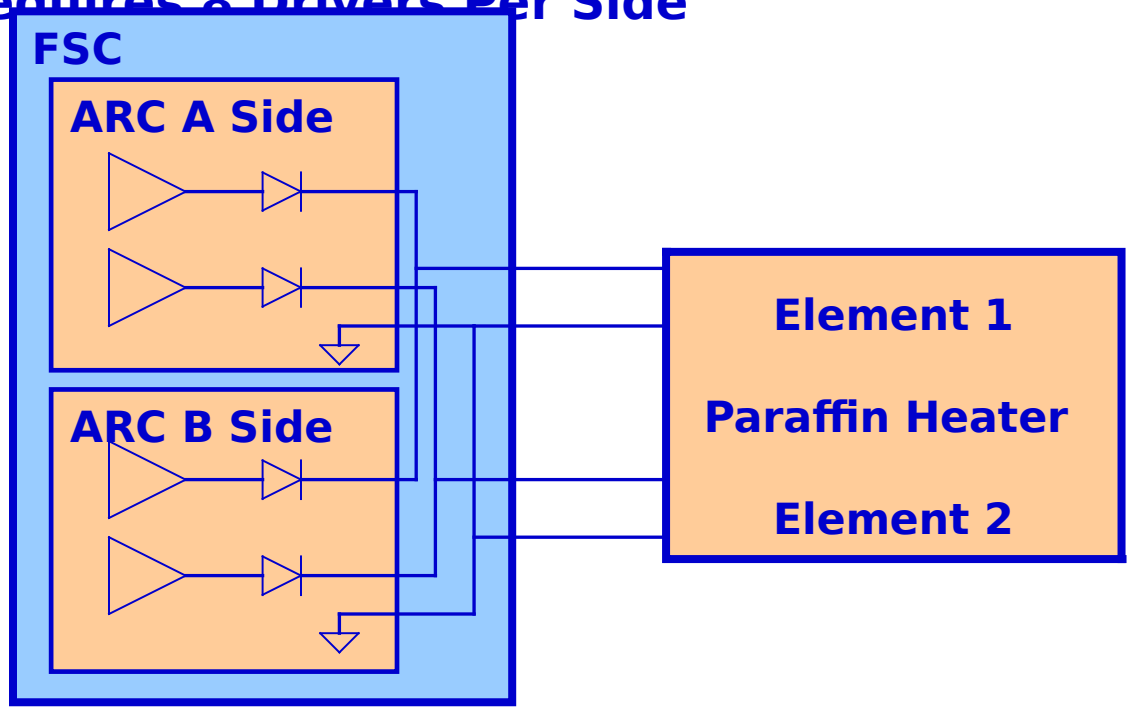
ARC Cross-Strapping 2 of 6

Latch Valve Cross-Strapping Requires 2 Drivers Per Side



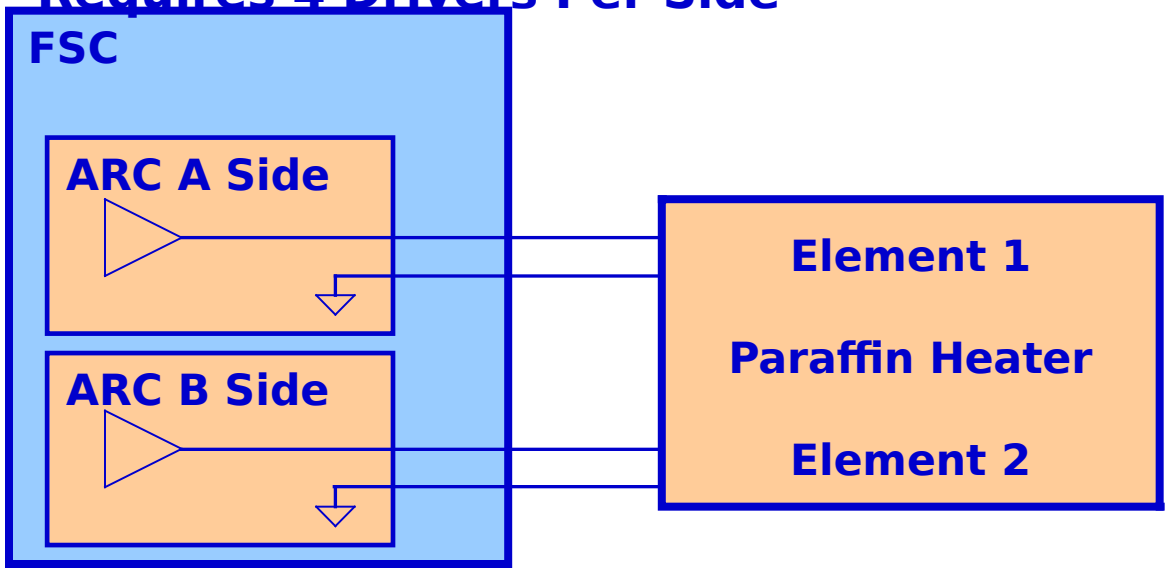
ARC Cross-Strapping 3 of 6

Paraffin Heater Cross-strapping Option A (One of Four Heaters Shown)
Requires 8 Drivers Per Side



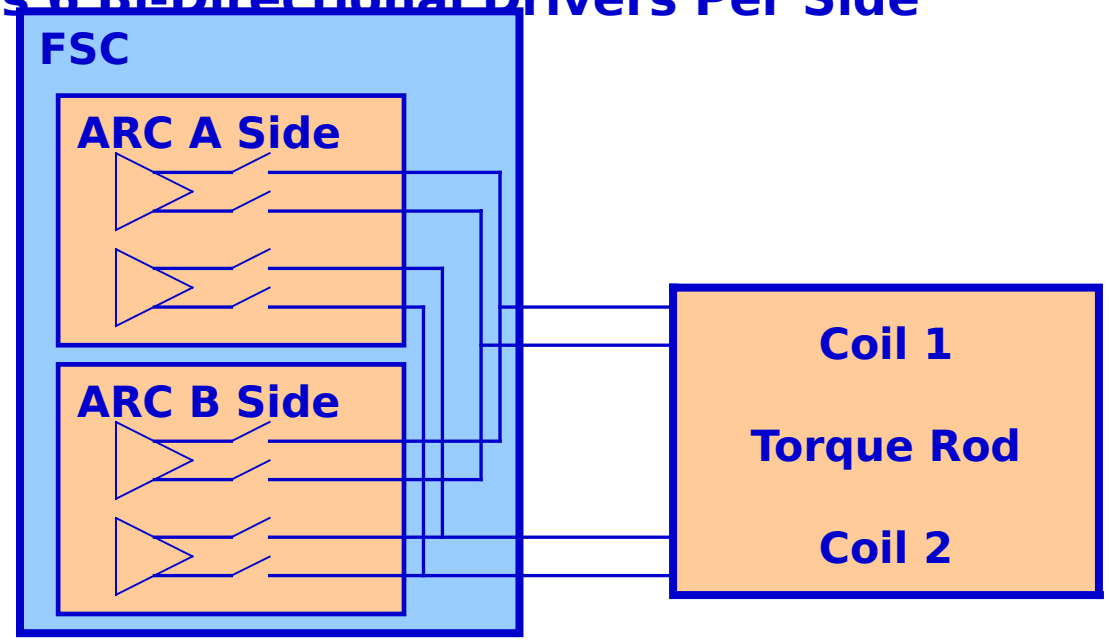
ARC Cross-Strapping 4 of 6

Paraffin Heater Cross-strapping Option B (One of Four Heaters Shown)
Requires 4 Drivers Per Side



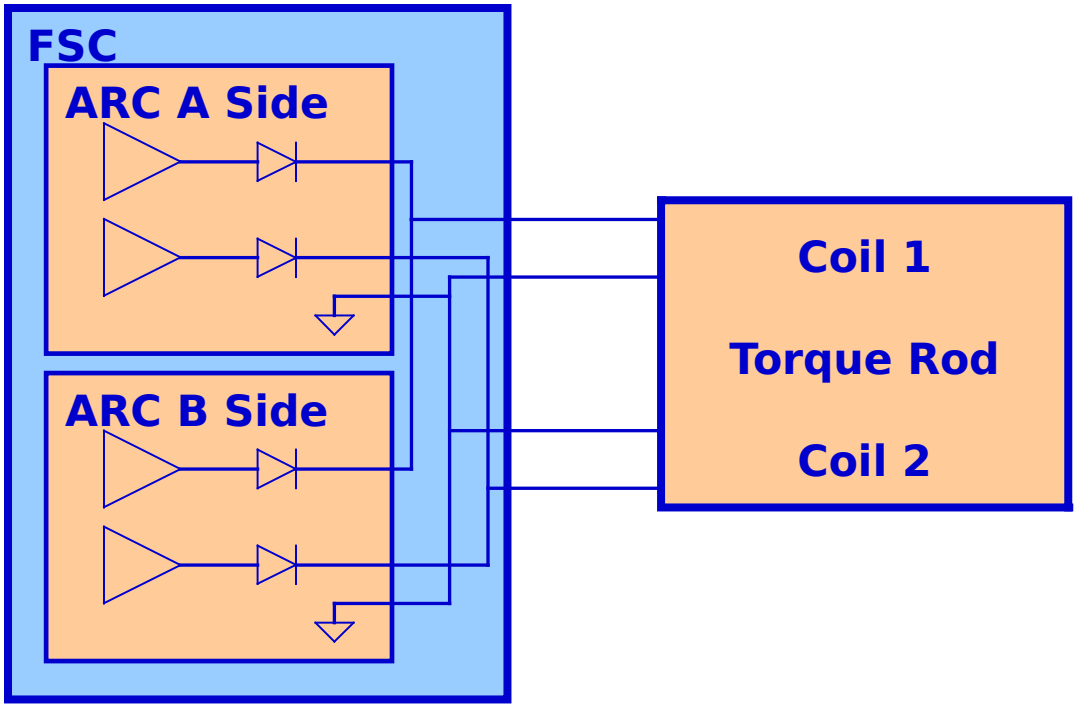
ARC Cross-Strapping 5 of 6

Torque Rod Cross-strapping Option A (One of Three Rods Shown)
Requires 6 Bi-Directional Drivers Per Side



ARC Cross-Strapping 6 of 6

Torque Rod Cross-Strapping Option B (One of Three Rods Shown)
Requires 6 Uni-Directional Drivers Per Side



ARC Trades 1 of 2

- Torque Rod Driver Polarity
  - Bi-Directional
    - Cross-Strapping Requires Relay Isolation
    - Redundant Torque Rod Coils Used As A and B
  - Uni-Directional
    - Cross-S Rod Coils Used As Forward and Reverse
- Torque Rod Driver Type
  - Current Controlled
    - Requires Three Separate Current Sources
      - Or Commanding of Only One Driver at a Time
    - Precise Moment Across Temperature Range
  - Voltage Controlled
    - Requires Unique Voltage Level
    - Heritage Driver Circuit

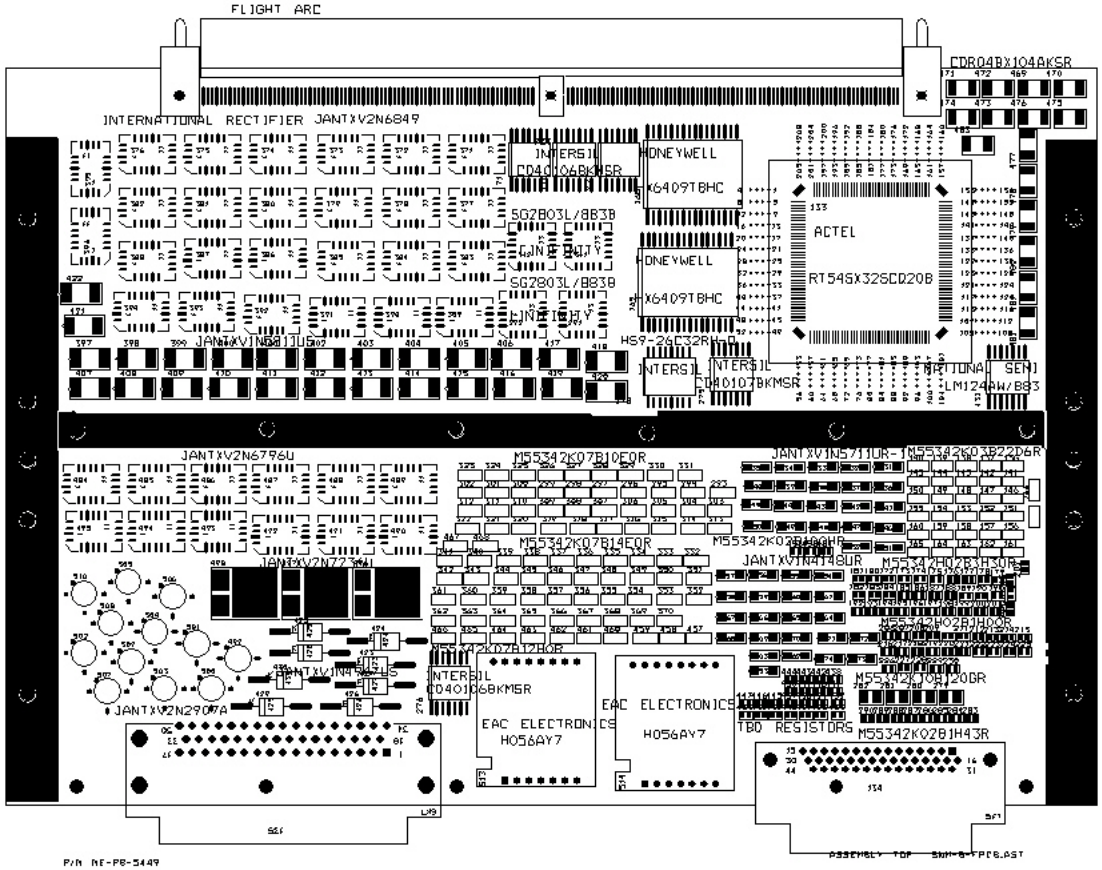
ARC Trades 2 of 2

- **Torque Rod Driver Control**
  - **Proportional**
    - **This Level of Control Not Required**
    - **Complex Circuit Design**
  - **On/Off**
    - **Heritage Driver Circuit**
- **Driver Power Control**
  - **SSR**
    - **Cost Prohibitive**
  - **MOSFET Switch**
    - **Similar Circuit to the Heritage Driver Circuit**

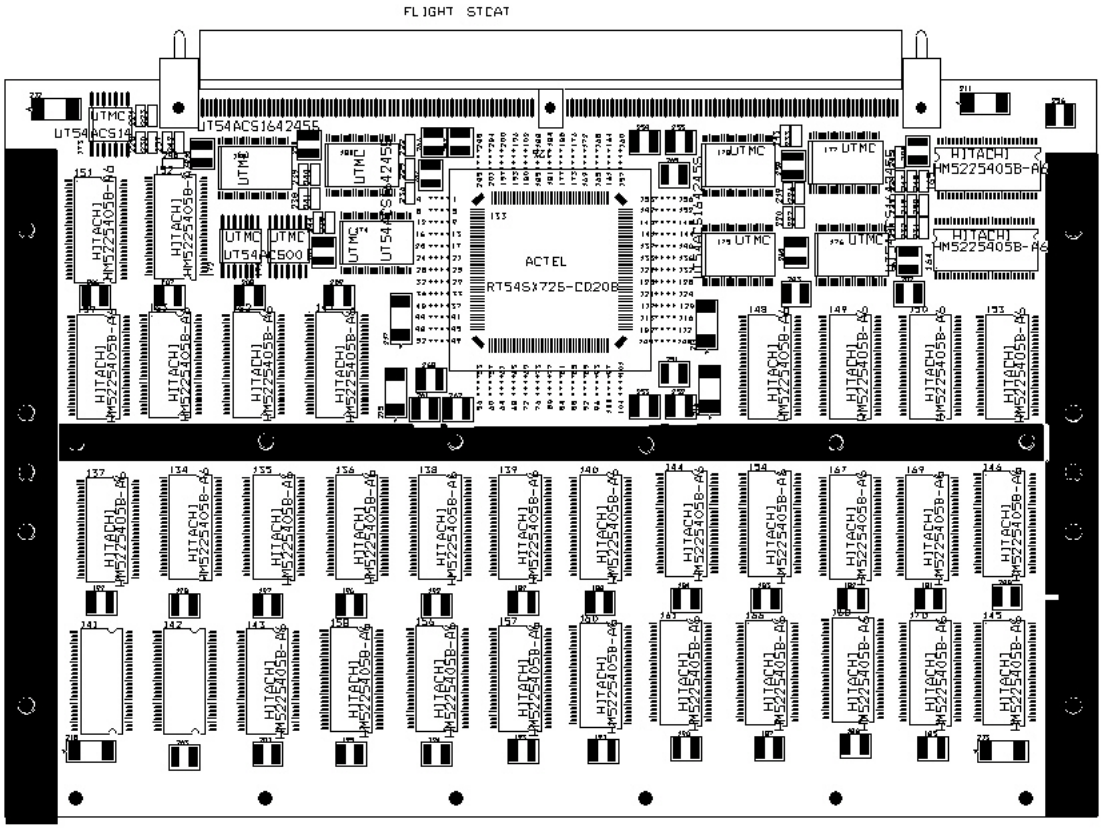
ARC Parts List

Item	Quantity	Part Number	Description	Package
1	1	RT54SX32SCQ256 alt: RT54SX32SCQ208 alt: RT54SX72SCQ256 alt: RT54SC72SCQ208	Actel FPGA	256 Pin Quad Flat Pack 208 Pin Quad Flat Pack 256 Pin Quad Flat Pack 208 Pin Quad Flat Pack
2	32	M55342K03B22D6R	22.6 Ohm	Chip - RM1005
3	2	HX6409TBHC	4096 x 9 Honeywell FIFO	32 Pin Flat Pack
4	4	CD40106BKMSR	CD40106	14 Pin Flat Pack
5	34	M55342H02B3H30R	3.3K Ohm	Chip - RM0505
6	25	M55342H02B1H00R	1K Ohm	Chip - RM0505
7	22	JANTXV1N5711UR-1	1N5711	Surface Mount
8	22	JANTXV1N4148UR-1	1N4148	Surface Mount
9	1	CD40107BKMSR	CD40107	8 Pin Flat Pack
10	1	HS9-26C32RH-Q	Differential Receiver	Flat Pack
11	4	M55342K10B120GR	120 Ohm	Chip - RM1010
12	8	M55342K02B1H43R	1.43K Ohm	Chip - RM0505
13	4	SG2803L/883B	Darlington Array	LCC - 20
14	39	D55342M07B10E0R	10K Ohm	Chip - RM1206
15	39	D55342M07B14E0R	14K Ohm	Chip - RM1206
16	26	JANTXV2N6849U	IRFE9130 Enhancement Mode P-FET	LCC - 18
17	26	JANTXV1N5811US	1N5811	Surface Mount
18	8	JANTXV1N4967US	1N4967	Surface Mount
19	1	LM124AW/883	5V Op-Amp	14 Pin Flat Pack
20	22	TBD	TBD Resistors	Chip - RM0505
21	3	M55342E02B100HR	100K Ohm	Chip - RM0505
22	12	D55342M07B12H0R	12K Ohm	Chip - RM1206
23	12	JANTXV2N2907A	2N2907A	TO-18
24	12	JANTXV2N6796U	IRFE130 Enhancement Mode N-FET	LCC - 18
25	2	H056AY7	Isolation Relay Contacts	Thru-Hole
26	3	JANTXV2N7236U	IRFN9140 Enhancement Mode P-FET	SMD-1
27	15	CDR04BX104AKSR	Bypass Capacitors - 0.1uF	Surface Mount
28	1	RM452-300-191-9501-900	300 pin AirBorn Connector	Surface Mount Edge
29	1	TBD	50 Pin D, low density	N/A
30	1	TBD	44 Pin D, high density	N/A
31	1	TBD	50 Wire Flex Print	Surface Mount
32	1	TBD	44 Wire Flex Print	Surface Mount

ARC Module Layout



SCMB Layout



SCMB Status

- **Module Definitions From DDR Being Used to Implement Design**
- **Further Requirements in Development**
- **Hitachi (Elpida) HM5225405B-A6 256mbit SDRAM for Flight**
- **Issue**
  - **None Currently**

UDM Command Interfaces

- **38 High Level Commands**
  - **28V, 44 msec Pulsewidth**
  - **Intended to Drive Relay Circuits Involved in Critical Spacecraft Functions.**
  - **Length May Be Adjusted to User Needs Prior to Final Flight Build**
- **4 Low Level Commands:**
  - **5V, 192 usec Pulsewidth**
  - **Length May Be Adjusted to User Needs Prior to Final Flight Build**
- **2 Differential Commands**
  - **For Instrument Reset**
- **Motor Control**
  - **A Low Level Interface Intended to Allow Processor Direct Control of Eight Stepper Motors Used on the FAME Spacecraft**

Critical Commands (PDU, PCU,RIU and Internal FSC)

PDU

1. Xmtr A On (HL)
2. Xmtr A Off (HL)
3. Xmtr B On (HL)
4. Xmtr B Off (HL)

PCU

1. UV Det Off (HL)

RIU

1. RIU A On (HL)
2. RIU A Off (HL)
3. RIU B On (HL)
4. RIU B Off (HL)

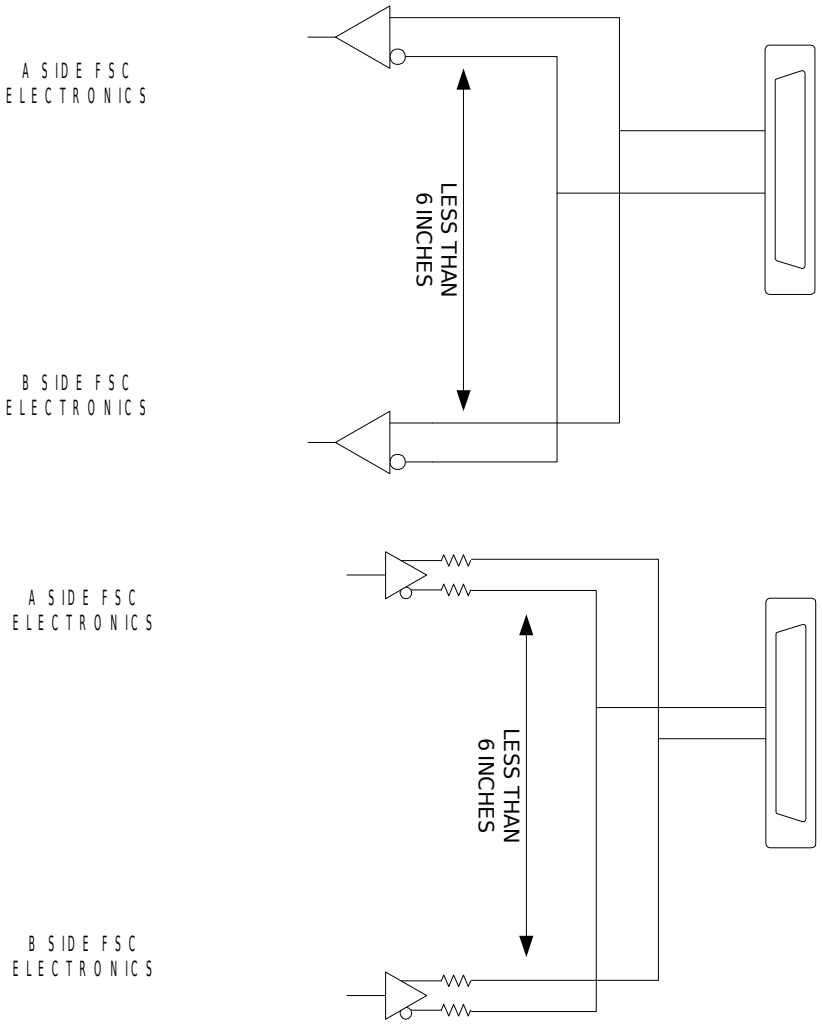
Internal to FSC

1. HSKPNG Supply A On (HL)
2. HSKPNG Supply A Off (HL)
3. HSKPNG Supply B On (HL)
4. HSKPNG Supply B Off (HL)
5. Reset Processor A (LL)
6. Reset Processor B (LL)
7. Alt Boot A (LL)
8. Alt Boot B (LL)

Transponder Critical Commands (All High Level)

1. Transmitter A On/B Off
2. Transmitter B On/A Off
3. Transmitter A Off/B Off
4. A Ranging On
5. A Ranging Off
6. B Ranging On
7. B Ranging Off
8. A Coherent Mode
9. A Non-Coherent Mode
10. B Coherent Mode
11. B Non-Coherent Mode
12. A Subcarrier On
13. A Subcarrier Off
14. B Subcarrier On
15. B Subcarrier Off
16. A Hi-Rate On
17. A Hi-Rate Off
18. B Hi-Rate On
19. B Hi-Rate Off
20. Antenna Transfer Switch Normal
21. Antenna Transfer Switch Inverted
22. SPT1 GTO Mode
23. SPT1 Mission Mode
24. SPDT2 GTO Mode
25. SPDT2 Mission Mode

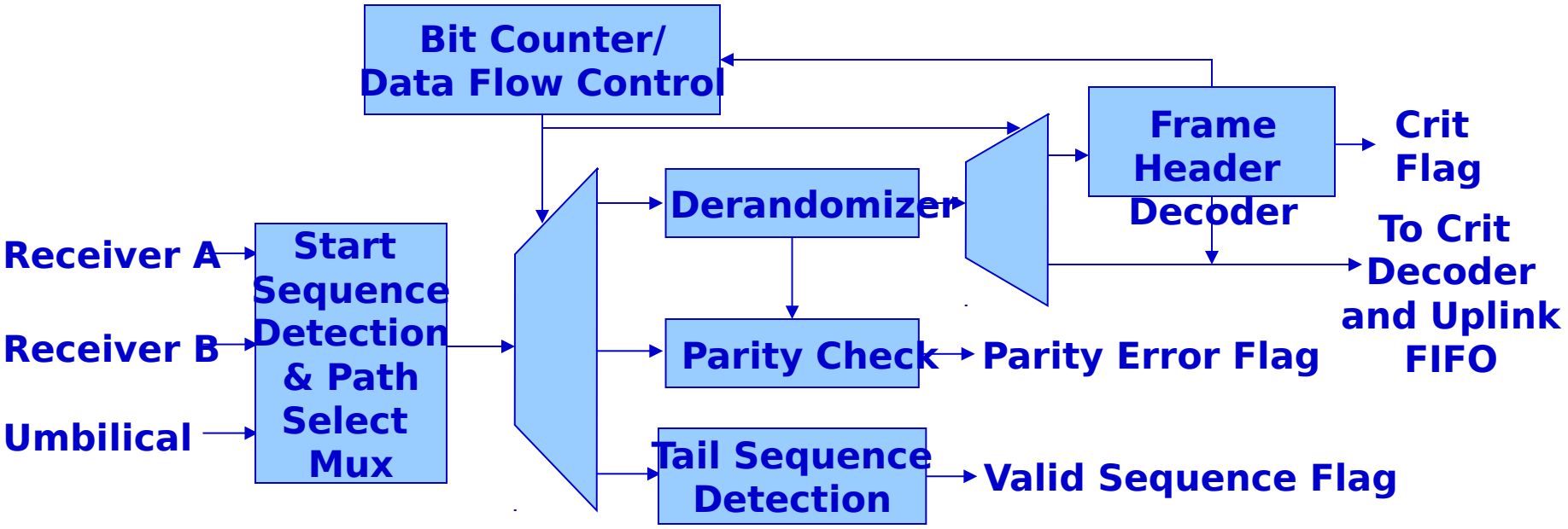
UDM Transponder Interface



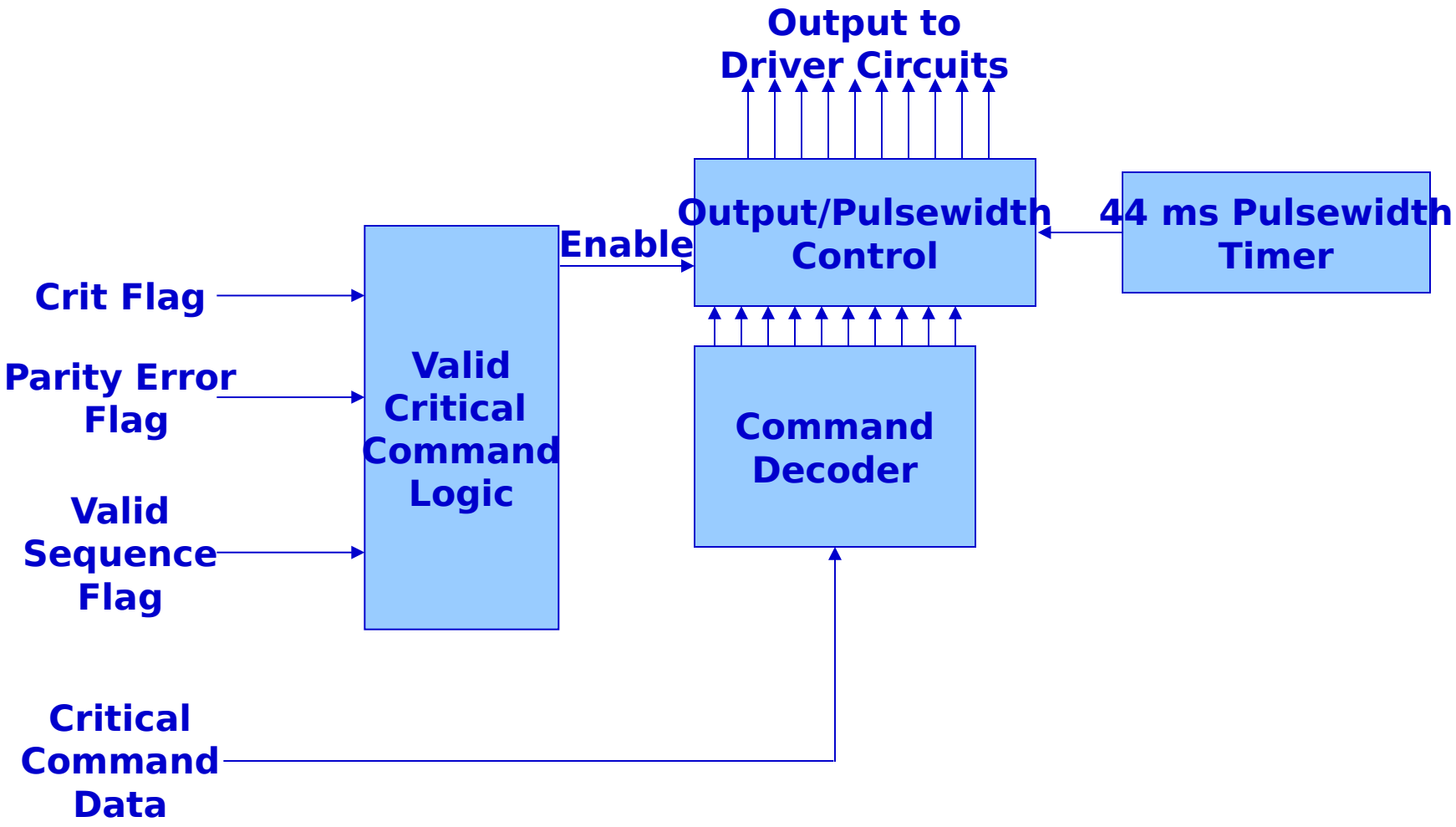
Uplink from Receiver A

To Transmitter A

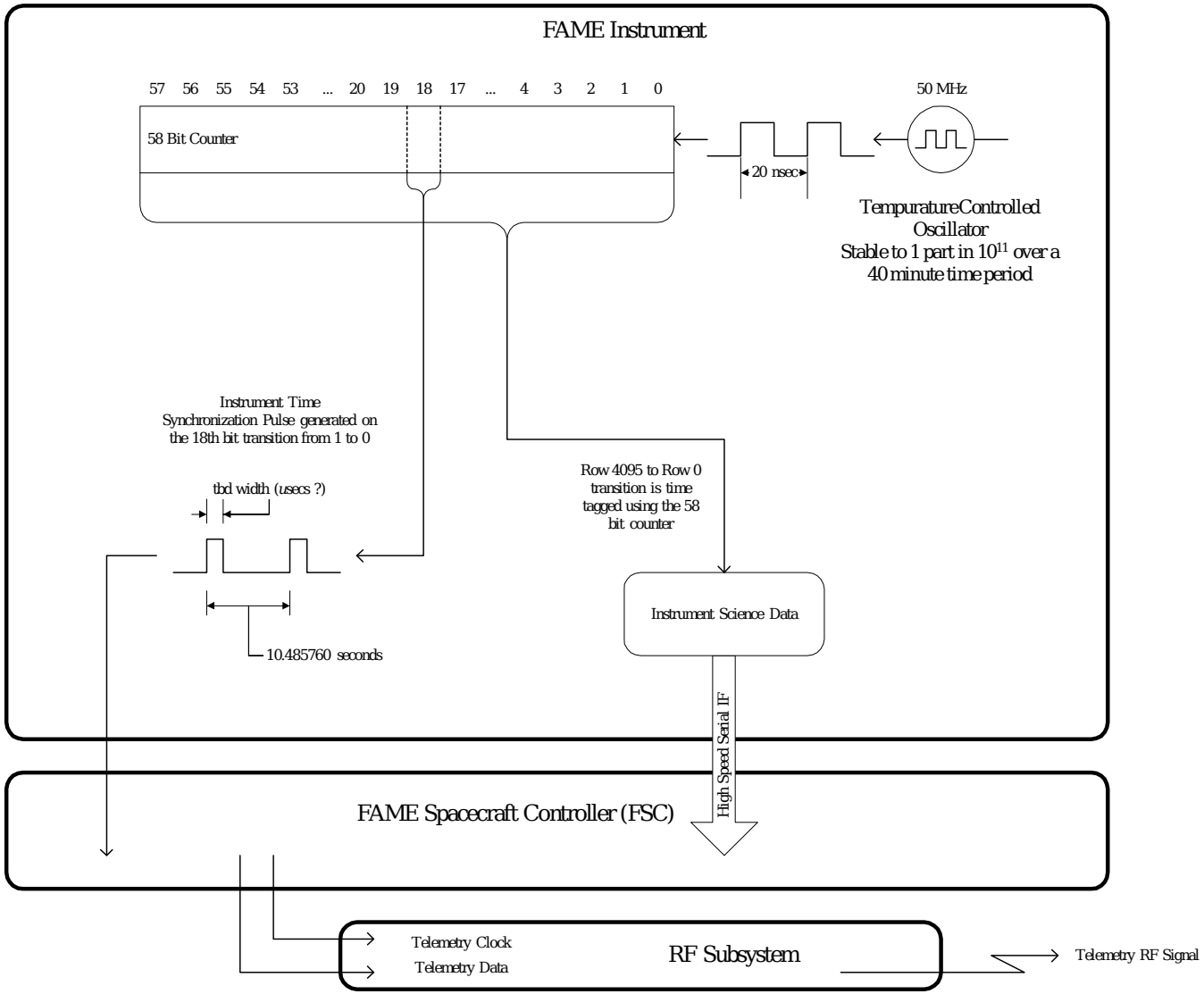
Uplink Module



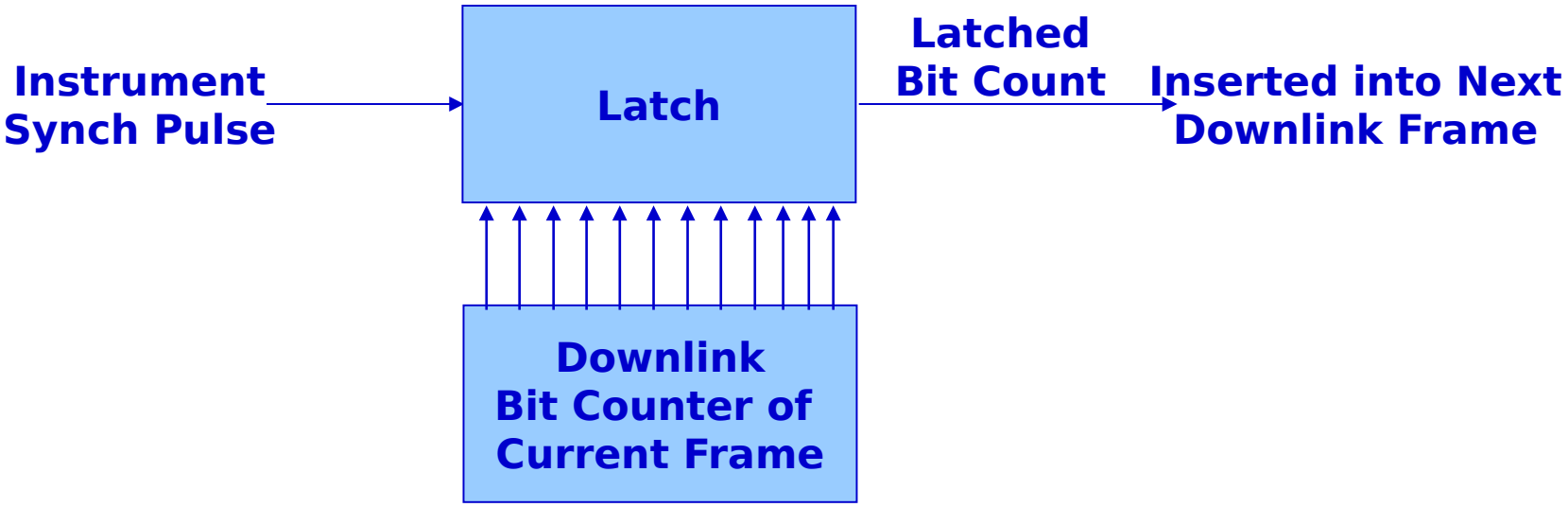
Critical Command Decoder



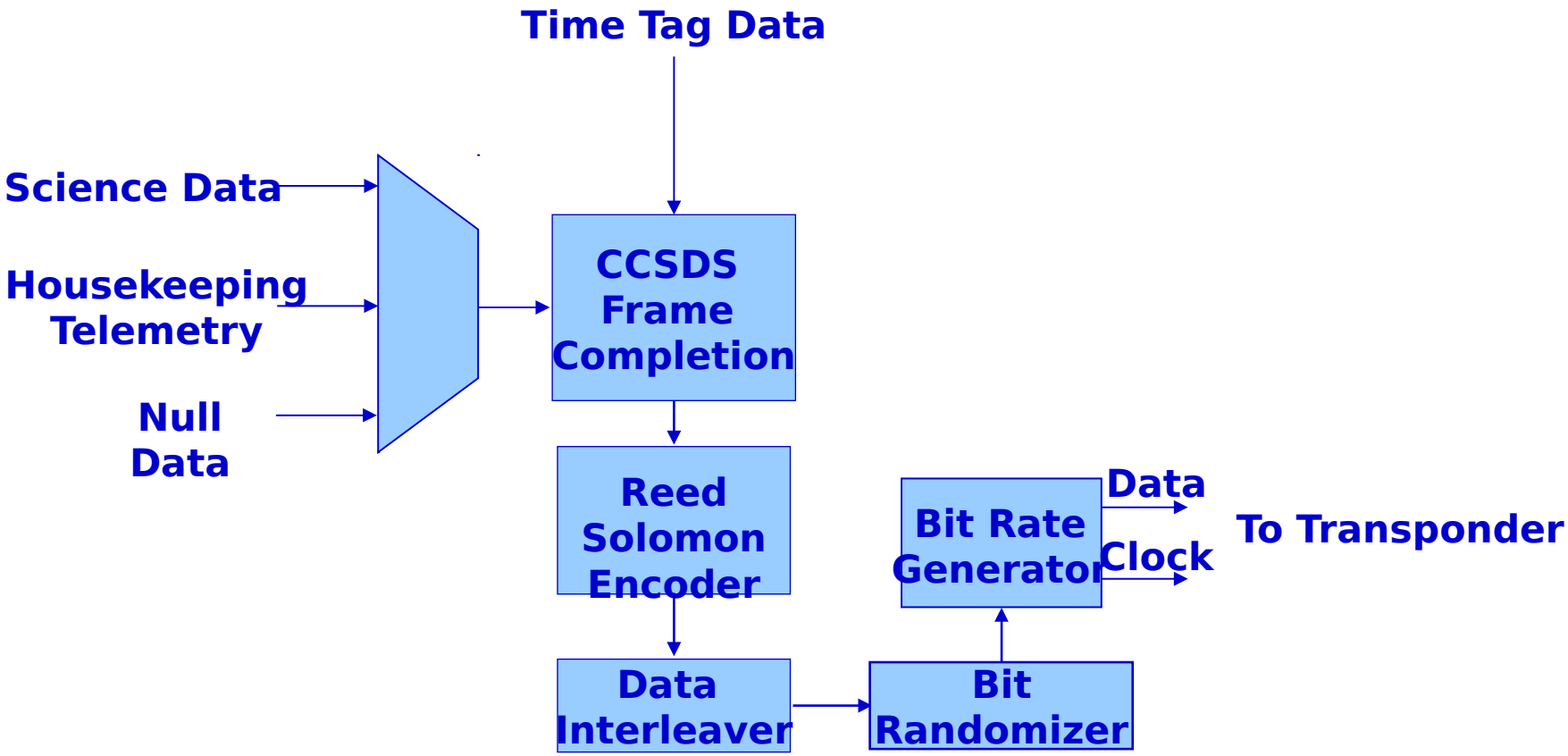
Instrument Synch Pulse



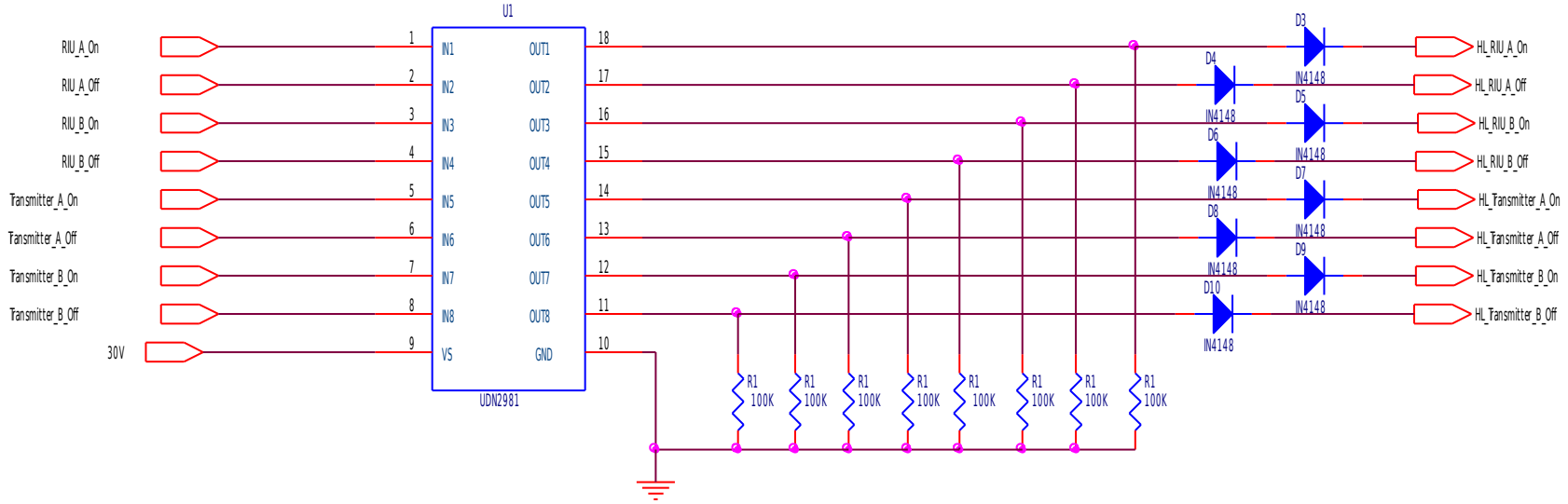
Instrument Downlink Synch Module



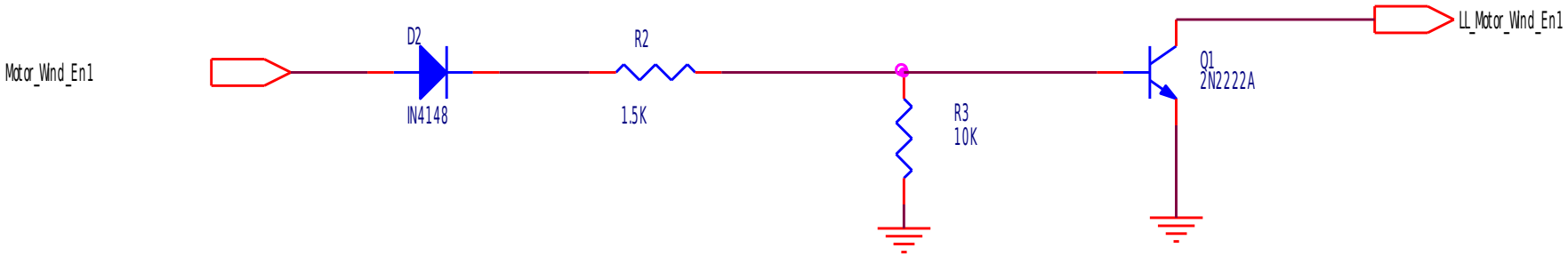
Downlink Module



Hi-Level Driver Circuit



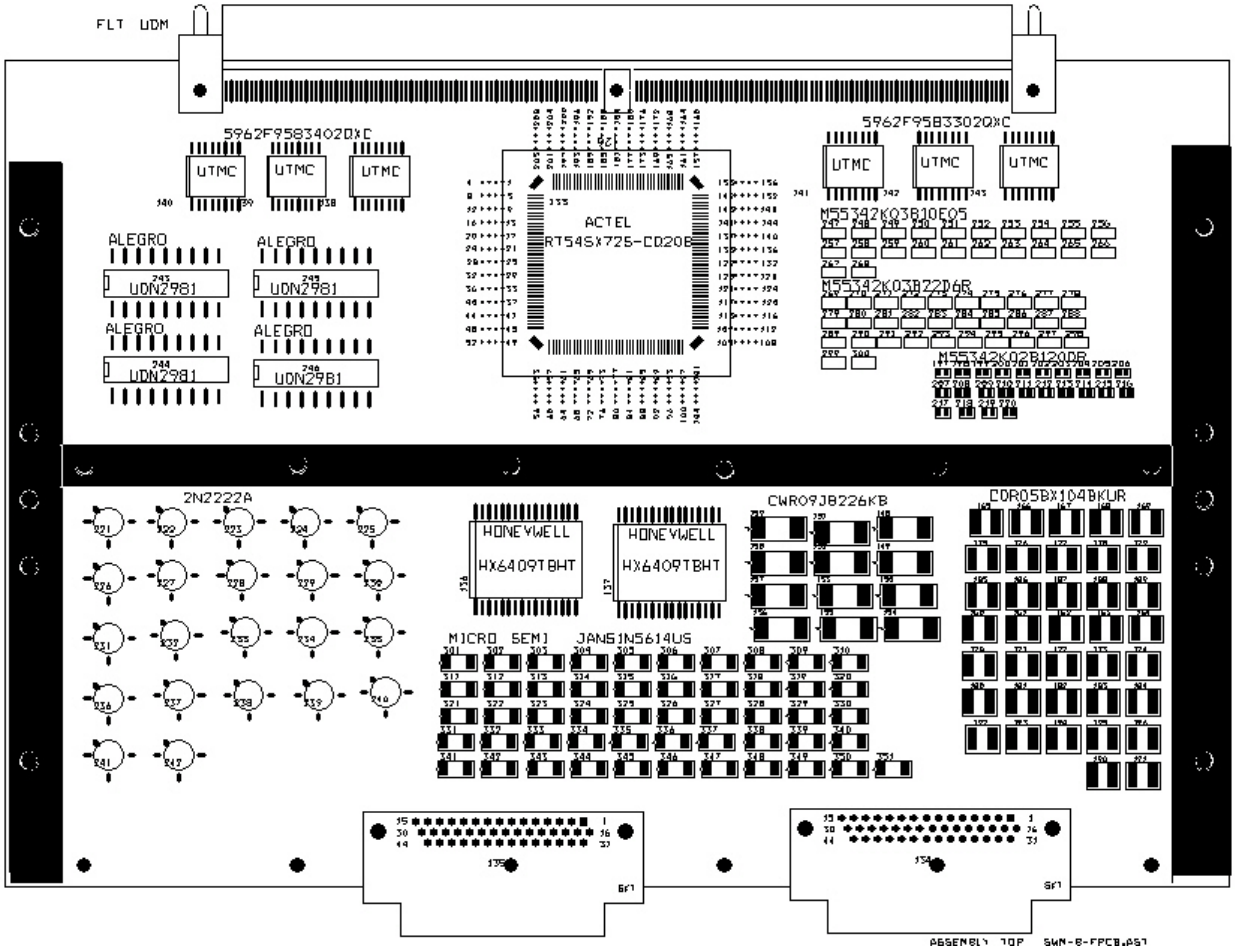
Motor Driver Circuit



UDM Parts List

Item	Quantity	PartNumber	Description	Manufacturer
1	12	CWR09JB226KB	Capacitor, 22UF_TANT, 20V	
2	37	CDR05BX104BKUR	Capacitor, 0.1uF, 10%, 100V	
3	24	M55342K02B120DR	Resistor, 120, 1%, 250mW	
4	3	5962F9583402QXC	LVDS, receivers	UTMC
5	2	311P407-3S-B-12	44 socket, D Connector	AMP
6	1	RM452-300-191-9501-9	300 Pin Edge Connector	AirBorn
7	22	M55342K03B10E05	Resistor, 10K, 1%	
8	2	HX6409TBHT	FIFO, 4096 x 9	Honeywell
9	3	5962F9583302QXC	LVDS, drivers	UTMC
10	1	RT54SX72S-CQ208	FPGA	Actel
11	32	M55342K03B22D6R	Resistor, 22.6, 1%, 100mW	
12	4	UDN-2981	Relay Drivers	
13	22	2N2222A	Transistor	
14	51	IN3611	Diodes	
			Flex Print for connector interface	

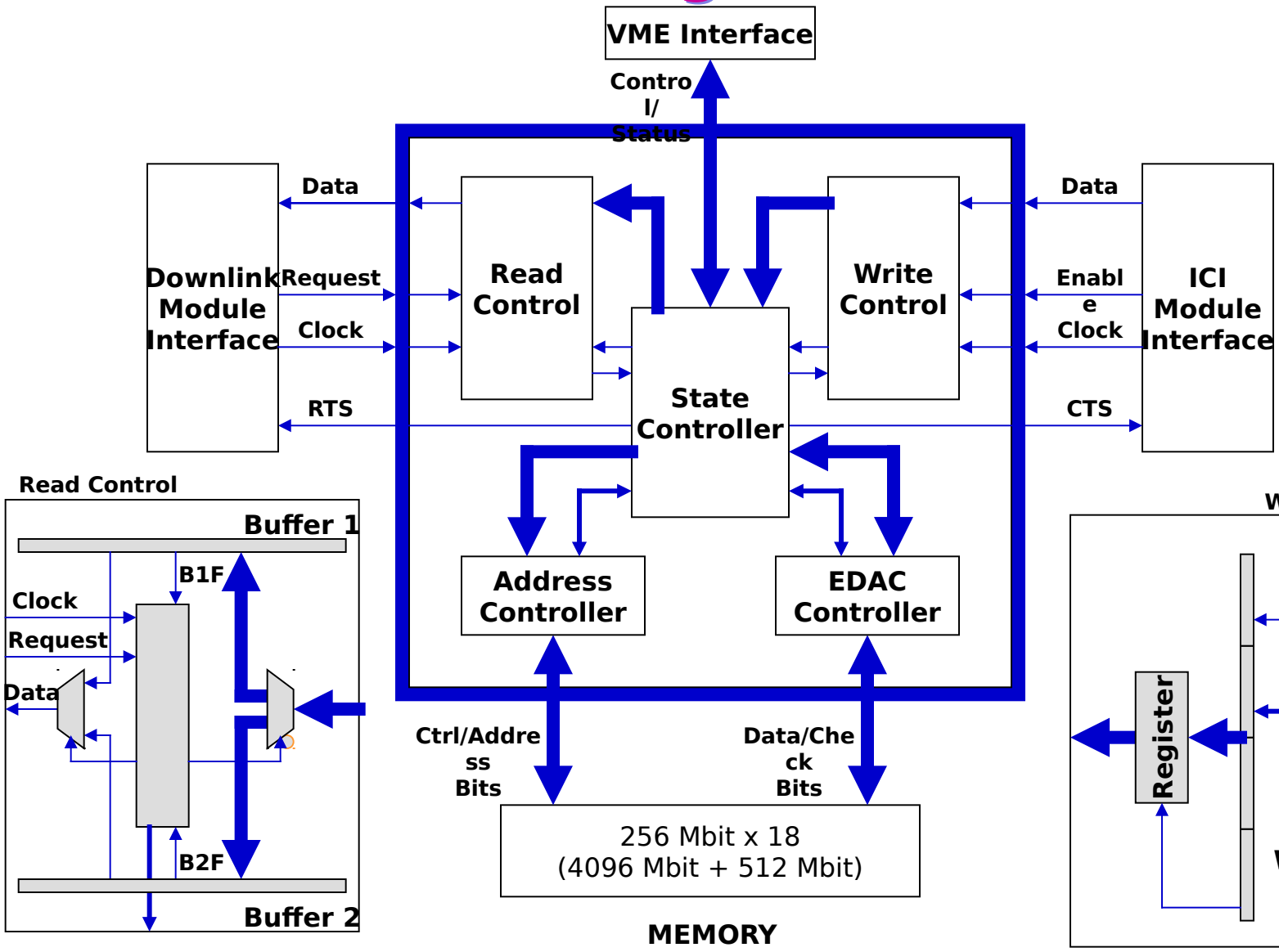
UDM Layout


FLT UDM
5962F9583402DXC
UTMC
UTMC
UTMC
ALEGRO
UDN2981
ALEGRO
UDN2981
ALEGRO
UDN2981
ALEGRO
UDN2981
ACTEL
RT54SX72S-CQ208
5962F9583302QXC
UTMC
UTMC
UTMC
M55342K03B10E05
M55342K03B22D6R
M55342K02B12D0R
2N2222A
HONEYWELL
HX6409TBHT
HONEYWELL
HX6409TBHT
CWR09JB226KB
CDR05BX104BKUR
MICRO SEMI JAN51N5614US
ASSEMBLY TOP SWN-8-FPCB.ASY

UDM Status

- **Uplink Module Simulated and Synthesized**
- **Breadboard Card Ready When VHDL Coding Is Finished**

DDR Detailed Block Diagram



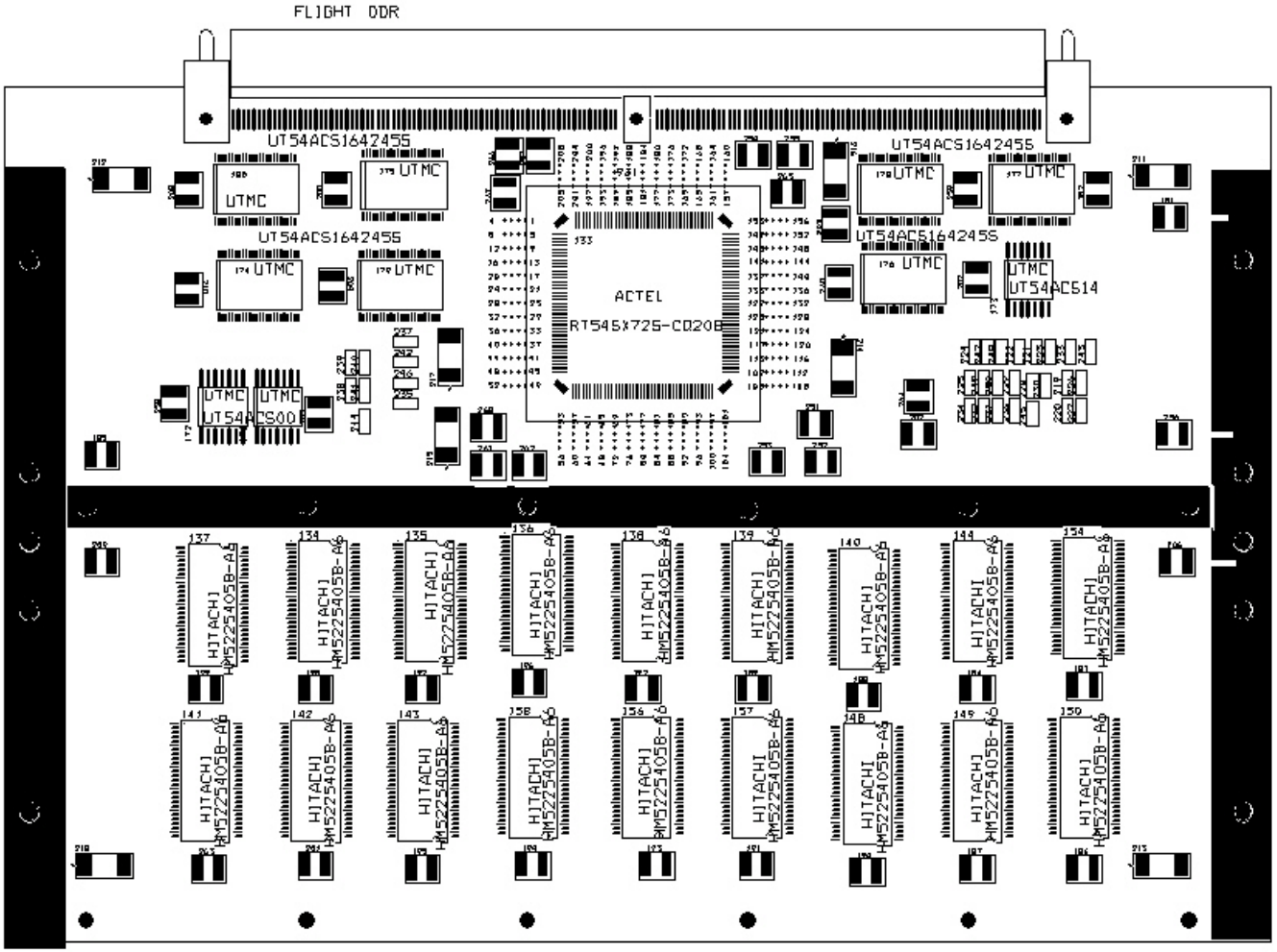
DDR Features

- **Error Detection and Correction (Hamming) Code Reduces SEU Effects in Memory**
- **Can Generate Statistical Data to Determine Current DDR SOH**
  - **Number of Single-Bit Errors Corrected**
  - **Number of Double-Bit Errors Detected**

DDR Parts List

1	RT54SX72S-CQ208	Actel	RadTolerant FPGAs for Space Applications	1
2	HM5225405B-A6 (?)	Hitachi (Elpida)	256Mbit LVTTL interface SDRAM	18
3	UT54ACS164245S	Aeroflex UTMC	RadHard Schmitt CMOS 16-bit Bidirectional MultiPurpose Transceiver	7
4	UT54ACS00/UT54ACTS00	Aeroflex UTMC	Radiation-Hardened Quadruple 2-Input NAND Gates	2
5	UT54ACS14/UT54ACTS14	Aeroflex UTMC	Radiation-Hardened Hex Inverting Schmitt Triggers	
7	CDR05BX104BKUR		Capacitor, 0.1uF, 10%, 100V	46
8	M55342K03B22D6R		22.6 ohm 1% Resistors	32
9	CWR09JB226KB		Capacitor, 22UF_TANT, 20V	6
10	RM452-300-191-9501-9xx		300 Pin Edge Connector	1

DDR Layout


FLIGHT DDR
UT54ACS1642455
UTMC
UT54ACS1642455
UTMC
UT54ACS1642455
UTMC
UT54ACS1642455
UTMC
UTMC
UT54ACS514
UTMC
UTMC
UT54ACS00
ACTEL
RT545X725-CQ208
HITACHI
HM5225405B-A6

DDR Status

- Initial Memory Testing Complete
- Sub-module Integration Complete
- VME Control and Testing Framework Complete
- Identification of Testing Modes Is On-Going
- Reduction in Control Logic Complexity Is On-going
- Hitachi (Elpida) HM5225405B-A6 256mbit SDRAM for Flight
- Issue
  - ACTEL 54SX72-S208 Selected As Flight Part Necessitating Reduction in Pin Count
  - Efforts Continue to Make VHDL Modules More Efficient

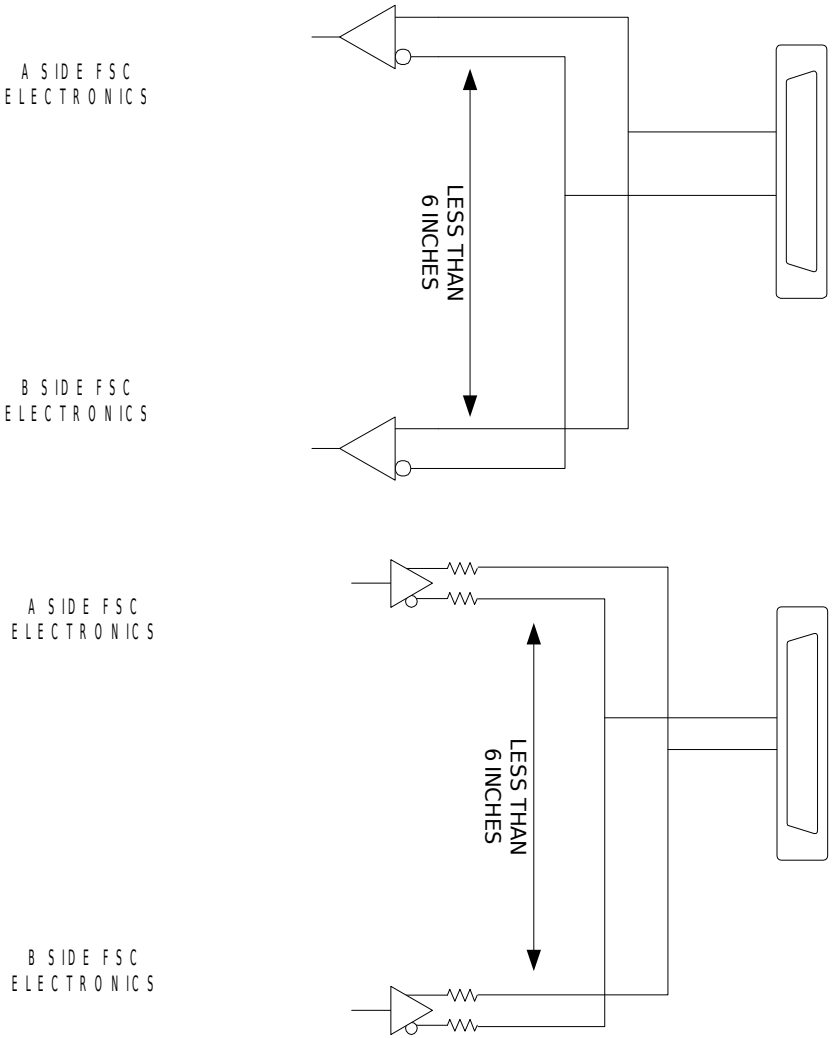
Memory Radiation Data

- **SEL Testing**
  - **Xe (Let=61 mev/mg/cm^2); V_{cc}=3.6v; >10^7 Particles**
    - **No Latchup @ 25°C**
    - **Power Down Clearable Latchup @ 70°C**
      - **Cross-Section: 1e-7 Cm^2/device**
  - **Kr (Let=35 mev/mg/cm^2); V_{cc}=3.6v; >10^7 Particles**
    - **No Latchup @ 70°C**
- **SEU Testing**
  - **25°C; V_{cc}=3.0v; > 4x10^6 Particles**
    - **Kr (LET= 35 mev/mg/cm^2) Cross-Section: 0.49 Cm^2/device**
    - **Ar (Let=10 mev/mg/cm^2) Cross-Section: 1.56e-3 Cm^2/device**
    - **C (Let=1.3 mev/mg/cm^2) Cross-Section: 9.82e-6 Cm^2/device**
- **Total Dose**
  - **V_{cc}=3.6V @ 80krad(si)**
    - **Fully Functional**
    - **V_{IL},I_{CC}: No Significant Change**

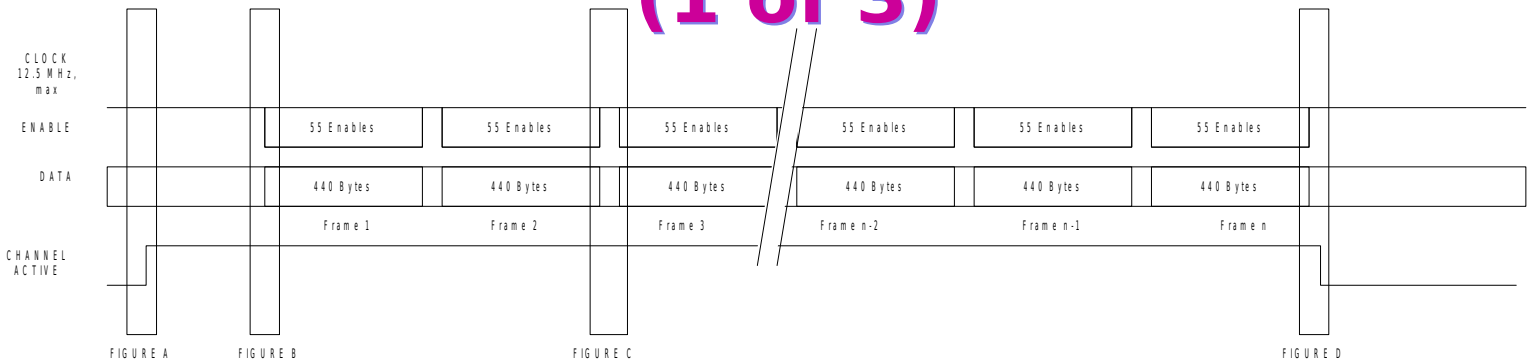
ACTEL Radiation Data

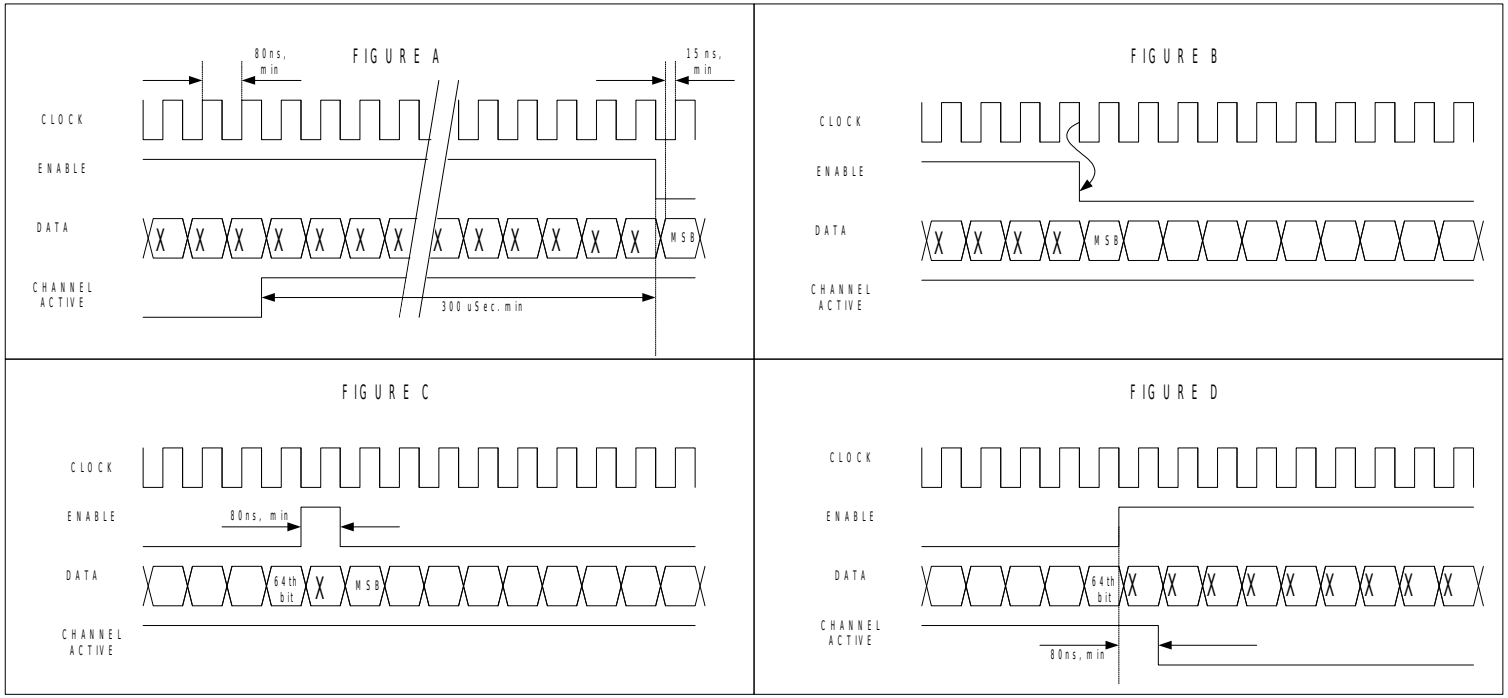
- LET_{th}> 40mev/mg/cm2, GEO SEU Rate <10^{-10} Upset/Bit-day)
- Up to 100krad (Si) Total Ionizing Dose (TID) Parametric Performance Supported With Lot-Specific Test Data
- Single Event Latch-Up Immune
- Tri-Stated Outputs at Power-Up
- Very Low Power Consumption (Up to 68 mW at Standby)
- 108,000 System Gates With 2,012 SEU Hardened Register Cells (Dedicated Flip-Flops)

ICI/Instrument Differential Interfaces

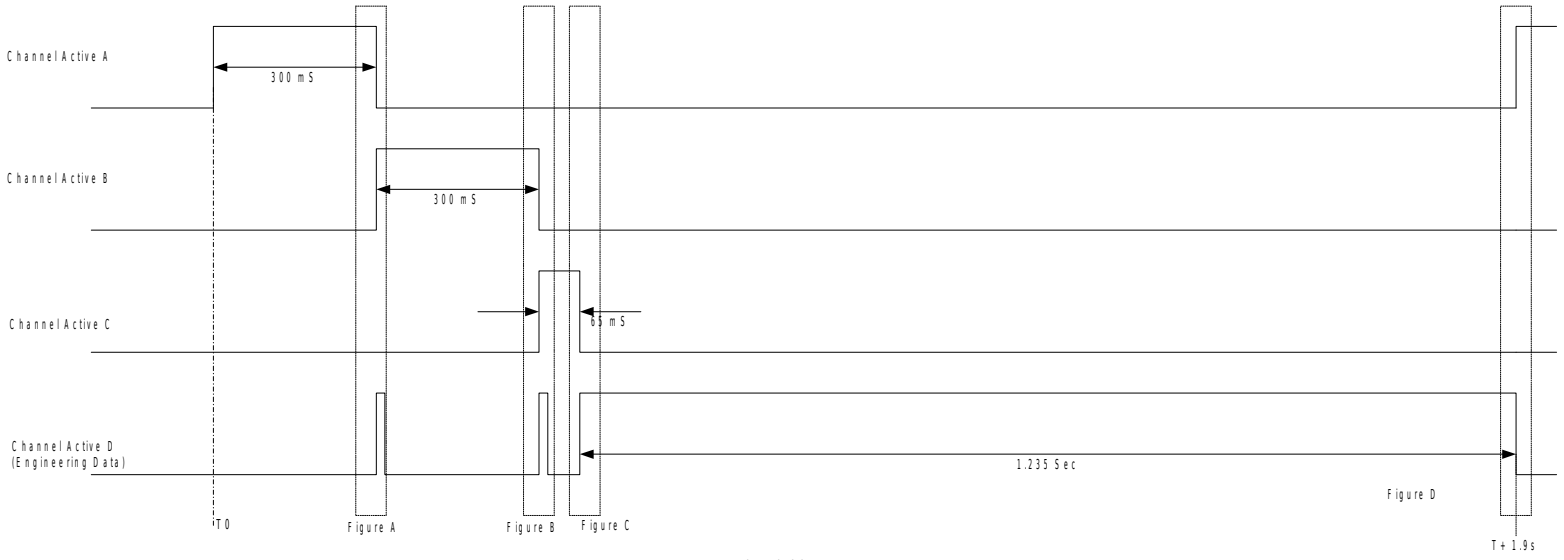


FAME Serial Bus (FSB) Timing (1 of 3)

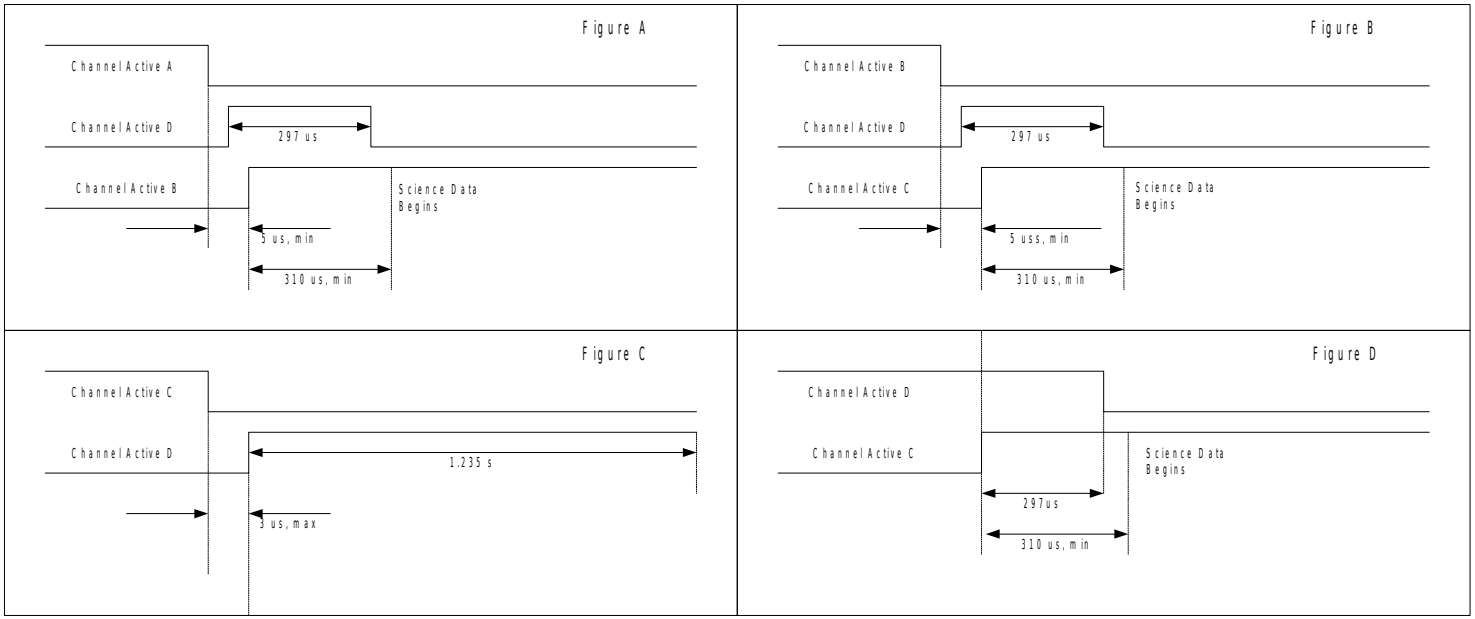




FSB Timing (2 of 3)



NOT TO SCALE



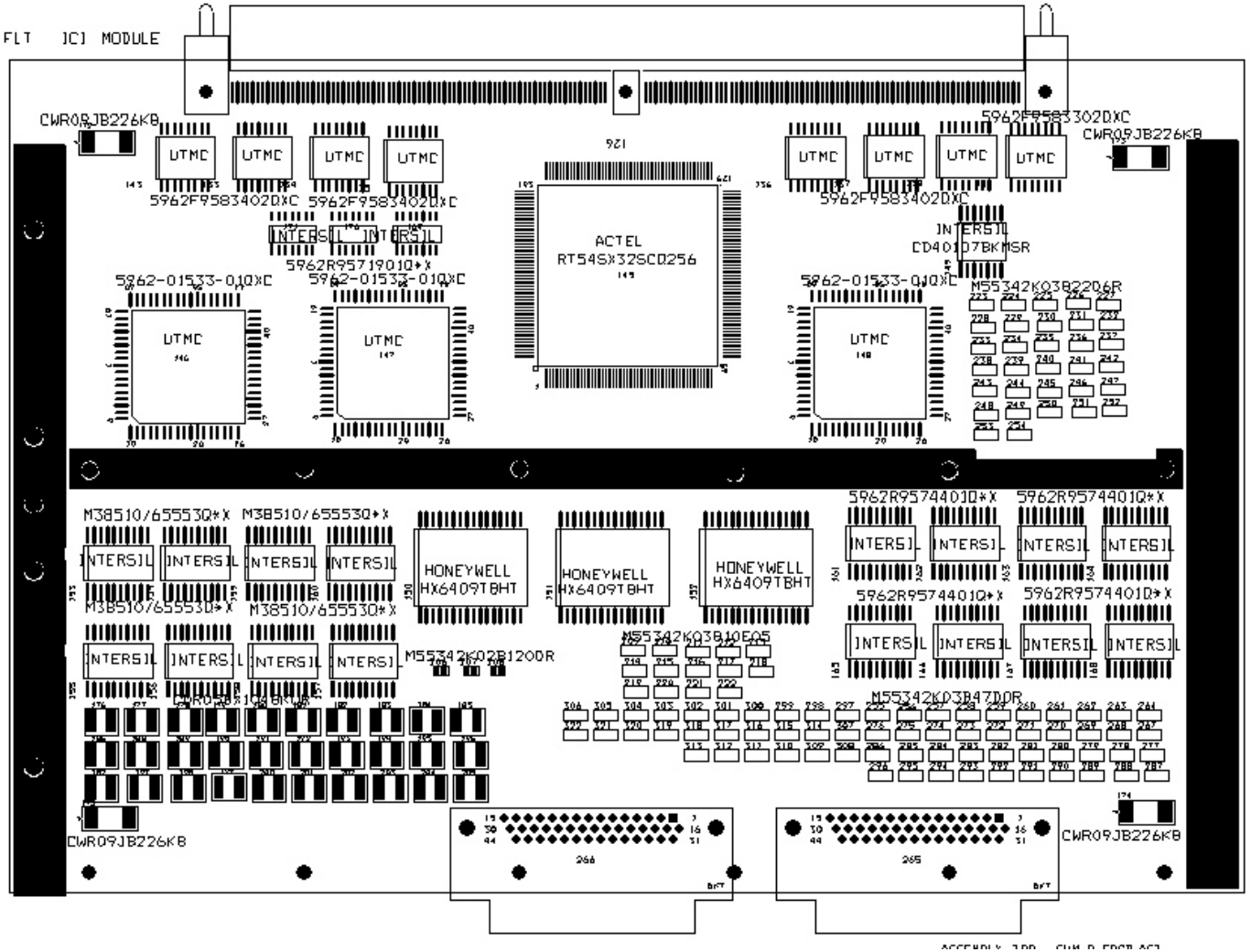
FSB Timing (3 of 3)

- 12.5 MHz Clock
- Data Latched on Rising Edge of Clock
- Enable Line Will Transition on Falling Edge of Clock
- Enable Brackets 64 Bits of Data
- Instrument Will Send Complete Frames of 440 Bytes
- Time From One Channel Active Removal to the Next Channel Active Assertion Is 5 Us, Minimum
- Following the Assertion of a Channel Active Signal, Data Will Not Start for a Minimum of 310 usec
- Only One Channel Active Signal Will Be Accepted at a Time
- All Channel Clocks Will Remain Active All the Time

ICI Parts List

Item	Quantity	PartNumber	Description	Manufacturer
1	4	CWR09JB226KB	Capacitor, 22UF_TANT, 20V	
2	30	CDR05BX104BKUR	Capacitor, 0.1uF, 10%, 100V	
3	3	M55342K02B120DR	Resistor, 120, 1%, 250mW	
4	7	5962F9583402QXC	LVDS, receivers	UTMC
5	2	311P407-3S-B-12	44 socket, D Connector	AMP
6	1	RM452-300-191-9501-9xx	300 Pin Edge Connector	AirBorn
7	14	M55342K03B10E05	Resistor, 10K, 1%	
8	3	HX6409TBHT	FIFO, 4096 x 9	Honeywell
9	3	5962-01533-01QXC	SRAM, 512K X 32	UTMC
10	1	5962F9583302QXC	LVDS, drivers	UTMC
11	8	M38510/65553Q*X	Bidirectional Buffer, Driver, HCTS 245	Intersil
12	3	5962R9571901Q*X	Receiver, Schmitt Trigger, HCTS14	Intersil
13	8	5962R9574401Q*X	Buffer, Driver, HCTS244	Intersil
14	1	RT54SX32SCQ256	FPGA	Actel
15	1	CD40107BKMSR	Open Collector Driver	Intersil
16	32	M55342K03B22D6R	Resistor, 22.6, 1%, 100mW	
17			Flex Print for connector interface	
18	66	M55342K03B47D0R	Resistor, 47, 1%, 100mW	

ICI Layout


FLT ICI MODULE
CWR09JB226KB
UTMC
5962F9583402DXC
INTERSIL
5962R9571901Q*X
5962-01533-01QXC
ACTEL
RT54SX32SCQ256
CD4017BKMSR
M55342K03B22D6R
M38510/65553Q*X
HONEYWELL
HX6409TBHT
5962R9574401Q*X
M55342K02B1200R
M55342K03B10E05
M55342K03B47D0R
266
265

FAME CT&DH Power Converter Input Power Requirements

- **Input Voltage Range**
  - **Normal Operation: 24 to 36 VDC**
  - **Survival: 0 to 40 VDC**
- **Internal Inrush Current Limiting for Compatibility With EPS Relays**
- **Conducted EMC (Per FAME EMC Control Plan and MIL-STD-461C)**
  - **Emissions Per MIL-STD-461 CE01, CE03. (FAME Limits)**
  - **Susceptibility Per MIL-STD-461 CS01, CS02, CS06 (FAME Limits)**

FSC Power Converter Output Requirements

Parameter	(Units)	UNSWITCHED OUTPUTS			SWITCHED OUTPUTS			
		2.5V	5.0V	30.0V	2.5V	3.3V	5.0V	30.0V (3)
Tolerance (1)	(±%)	5	5	15	5	5	5	N/A
Ripple	(mV p-p)	25	100	1000	25	30	100	N/A
Max. Current	(A)	0.15	0.50	0.23	0.75	2.60	3.05	0.09
Min. Current	(A)	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Max. Power	(W)	0.38	2.50	6.99 (2)	1.88	8.58	15.25	2.70

Notes: 1) Tolerance includes effects of ripple, noise, and all combinations of line, load and temperature conditions.
2) 28V output supplies relay and torque rod drive power. Load is pulsed.
3) 30V output is filtered unregulated bus power.

Load Power Totals (Max.)

Unswitched:	9.9W
Switched:	28.4W
Total:	38.3W (31.3W Steady State)

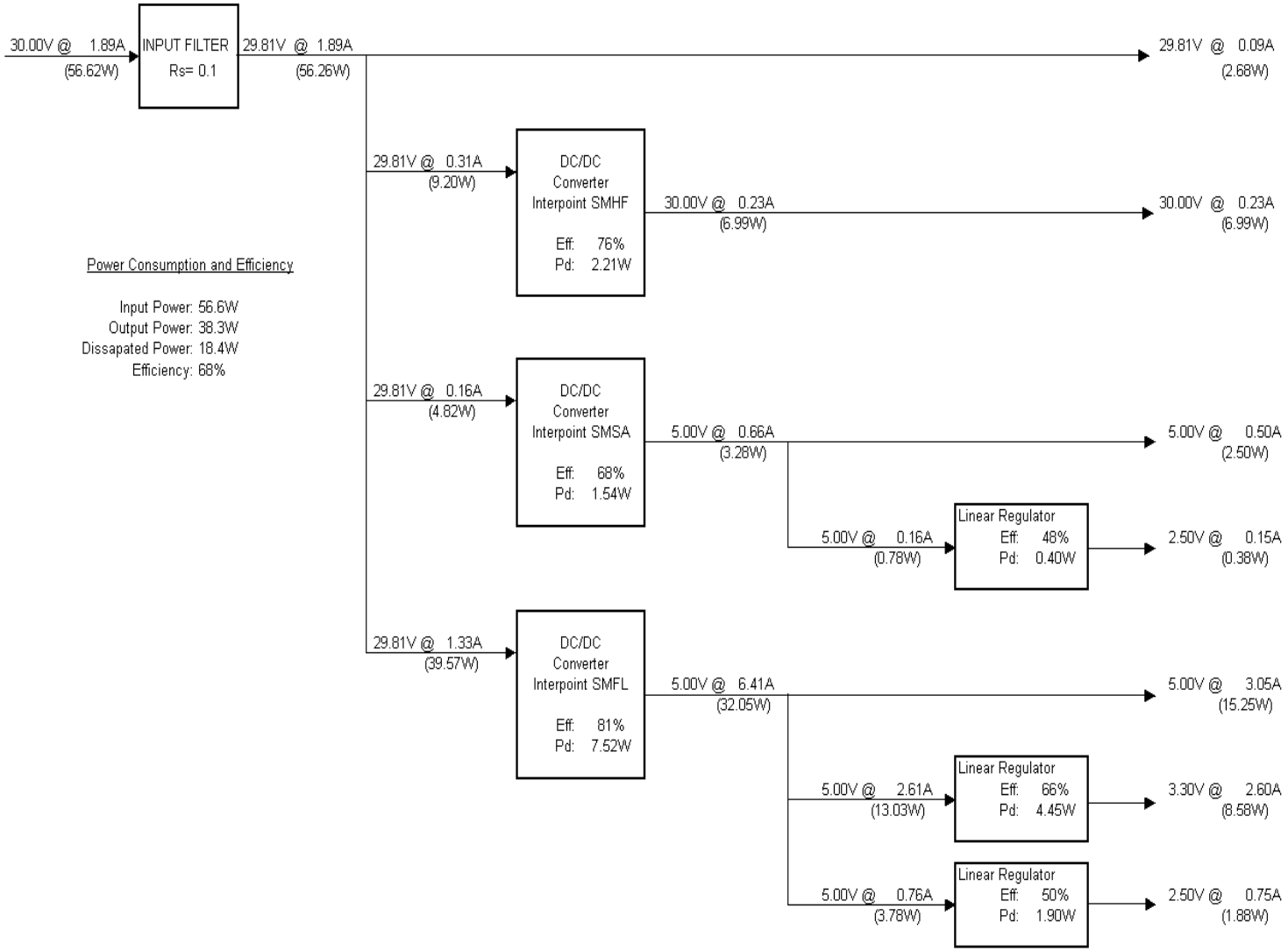
Power Converter Design Characteristics and Features

- Power Converter Topology: 3 DC/DC Modular Converters and 3 Linear Regulators Provide 6 Regulated Outputs. Unregulated Bus Power Also Provided to the Thrusters Through a Current Limited Output
- Power Converter Employs Interpoint DC/DC Converters to Achieve Reduced Design Effort and Cost
- Protective Features:
  - Input Undervoltage Lockout
  - Output Overload and Short Circuit Protection on All Outputs
- Latching Relay Command Interface for Converter ON/OFF Control
- Fabricated With Combination of Surface Mount and Through Hole Techniques

Power Converter Interpoint DC/DC Converter Modules

MODEL	INPUT VOLTAGE RANGE	OUTPUT VOLTAGE	OUTPUT CURRENT		RIPPLE VOLTAGE	
			RATED	REQUIRED	UNIT SPEC	REQUIRED
SMHF2815D	16 To 40 VDC	30V	0.5A	0.23A	550mV	1000mV Max.
SMSA2805S	16 To 40 VDC	5.0V	1.0A	0.66A	450mV	100mV Max.*
SMFL2805S	16 To 40 VDC	5.0V	10A	6.41A	50mV	100mV Max

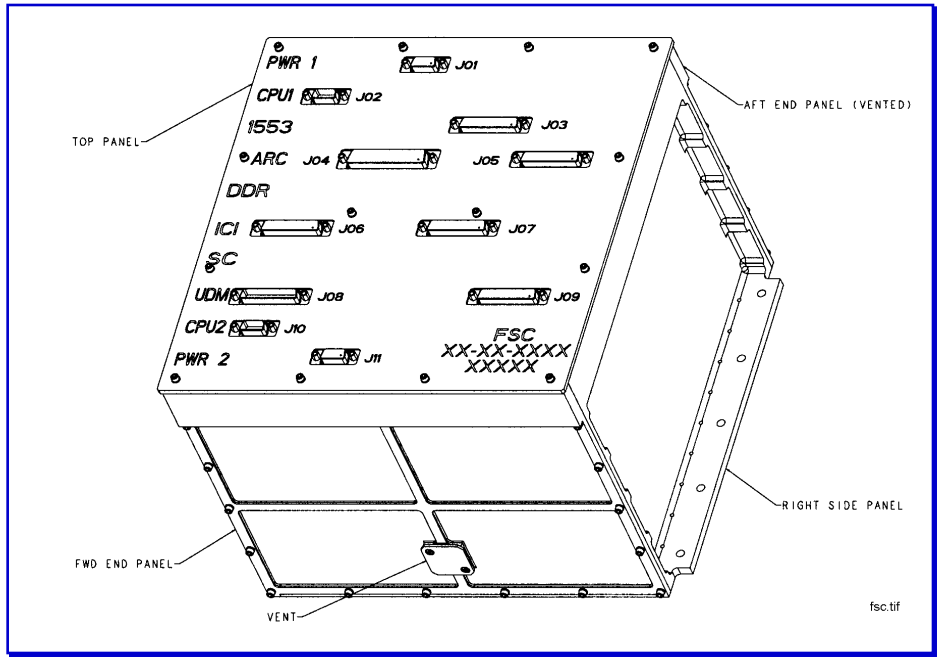
Power Converter Power/Efficiency Diagram

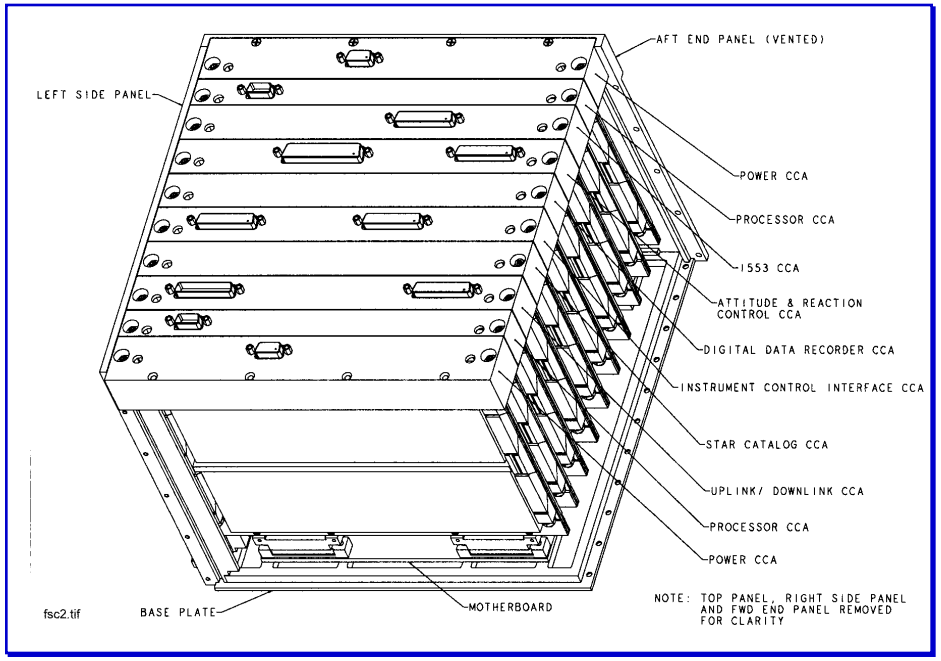


Power Consumption and Efficiency

Input Power: 56.6W
Output Power: 38.3W
Dissapated Power: 18.4W
Efficiency: 68%

FSC Mechanical Design





FAME Spacecraft Controller (FSC)

Estimated Mass and Power

- **FSC:**
  - **Mass: 31.9 Pounds**
  - **Power**
    - **Unswitched: 13 Watts**
    - **Switched: 23.5 Watts**
- **RIU:**
  - **Mass: 11.1 Pounds**
  - **Power**
    - **Nominal: 3 Watts**
    - **Peak : 7.3 Watts**

FSC Box-Level Test Approach

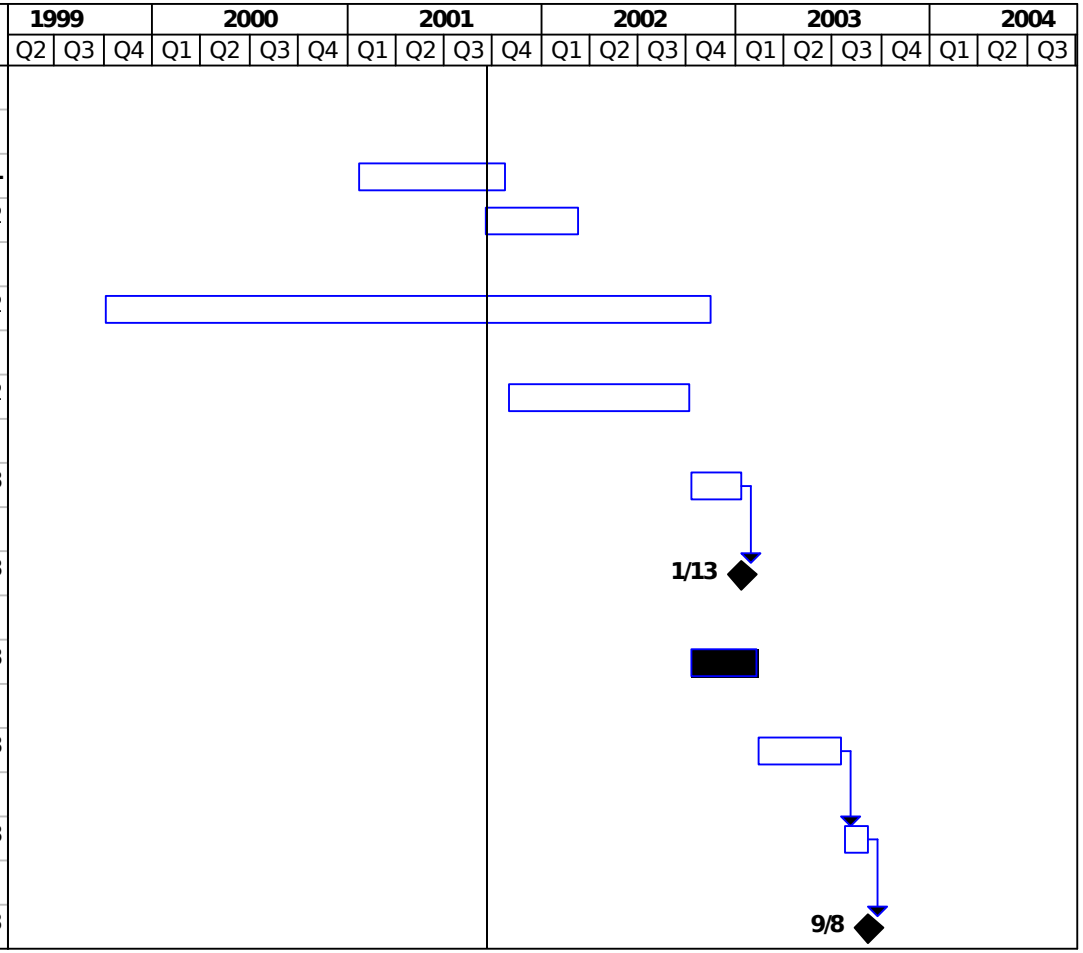
- **Module Level, Box Level, System Level - Use Similar Toolset**
- **Black Box Testing Based on Requirements and Interfaces**
- **White Box Testing for Areas of Risk**
- **Tests Completely Automated, Archived**
- **Qualification Level Testing on Brassboard FSC**
  - **Burn In, EMI/EMC, Random Vibe, Thermal, TVAC**
- **Acceptance Level Testing on Flight FSC**
  - **Same Tests Using Flight Levels (Slightly Lower Than Qual.)**
- **Testing at 24v, 30v, 36v**

ATP Areas to Test

- External Interfaces - Functional and Errors
- Simulation of All Phases of the Mission
- ADAC Testing - All Sensors, All Modes
- Instrument Testing - All States
- End to End Data Flow
  - Special Software Data Generators and Data Validation Tools Will Be Used to Insure That No Data Is Lost and That All Data Rates/Paths Are Exercised

Schedule Summary

ID	Task Name	Start	Finish
1			
2			
3	**Breadboard Build (all but StCat and Instrument I/F)**	**Fri 1/19/01**	**Fri 10/26/01**
4	Breadboard Build (StCat and Instrument I/F)	Fri 9/7/01	Mon 3/11/02
5			
6	S/C Processor Procurement	Mon 10/4/99	Fri 11/15/02
7			
8	Engineering Model Build	Mon 10/29/01	Fri 10/4/02
9			
10	Engineering Model Testing	Mon 10/7/02	Fri 1/10/03
11			
12	Deliver EM to NRL For Deck Testing	Mon 1/13/03	Mon 1/13/03
13			
14	Flight Model Build	Mon 10/7/02	Mon 2/10/03
15			
16	Flight Unit Testing	Tue 2/11/03	Fri 7/18/03
17			
18	Slack Time/Sched Reserve	Mon 7/21/03	Fri 9/5/03
19			
20	Deliver Flight Unit to Spacecraft	Mon 9/8/03	Mon 9/8/03



Peer Review Issues

- **Peer Review Occurred on October 16, 2001**
- **Issue 1: Cross-Strapping to UDM To/From Transponder Has Single Point Failures**
  - **Resolution (See CT&DH Backup, Page: 45)**
    - **Uplink Receiver Drives RS-422 Receivers in Parallel**
    - **Each Downlink Transmitter Can Be Driven Directly by Either UDM**
- **Issue 2: UDM High Level Command Driver Could Short Out 30V**
  - **Resolution (See CTDH PDR, Page 18)**
    - **30V DC/DC Converter Can Be Disabled**